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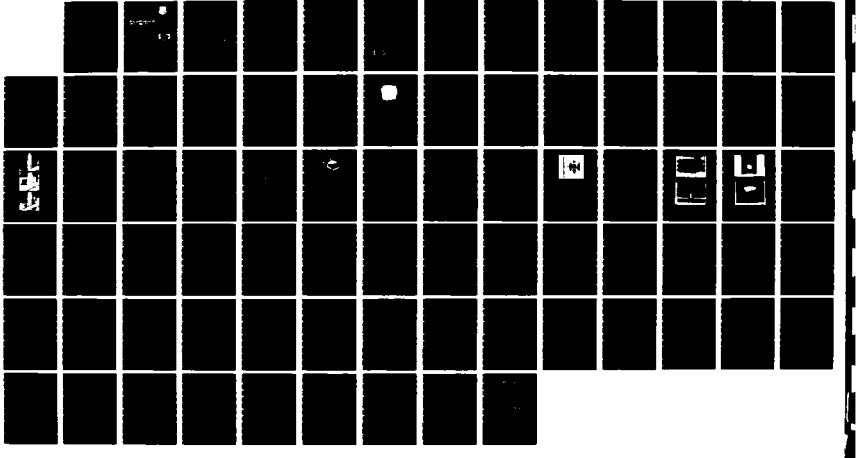

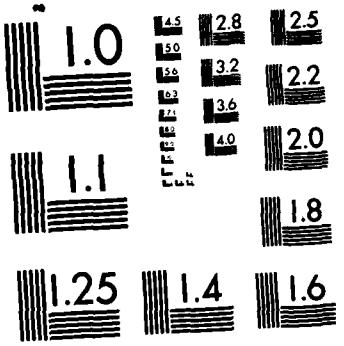

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Final Technical Report
September 1985

METALLIZATION QUALIFICATION FOR VLSI (TRACE TEST)

General Electric Company

Dr. Donald J. LaCombe and Mr. Earl L. Parks

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, NY 13441-5700

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The objective of this work was to define a standard test procedure to qualify VLSI metallization systems for government applications. The susceptibility of the metallization to electromigration was the primary concern of this qualification. Life tests were conducted in which a large number of test lines were stressed to failure. Resistance change was monitored and the correlation between rate of change and lifetime evaluated. It was determined that the correlation was small and therefore resistometric test methods are not suitable for predicting life. Finite element modeling of the resistance change process was used to explain some of the anomalous resistance variations which were observed.

The time to failure was found to be log-normally distributed down to the 0.2% failure point. It was also found that a very long test line is statistically equivalent to many shorter lines when evaluating early failures. Therefore, a lift test in which a modest number of very long lines are tested to failure is an efficient test for evaluating early failures.

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A draft of a standard test method, based on this approach, is included as an Appendix.

EVALUATION

This contract was well done by two conscientious investigators with excellent research backgrounds. The effort combined experimental data, statistical analysis and computer modeling to provide some new insights into the electromigration mechanism. Through this effort it is clear that large numbers of test patterns combined with accelerated test techniques are required to bridge the gap between awareness of a wearout failure mechanism and its control in large scale manufacturing operations and the subsequent field use of devices having such a wearout mechanism. Much more work is necessary, but this contract has set the stage for a standard method of obtaining and processing the data so that meaningful comparisons can be made relative to the effect of manufacturing and use variables on electromigration failure lifetime.

Clyde H. Lane

CLYDE H. LANE
Project Engineer

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We also acknowledge Mr. Clyde Lane of RADC for his guidance and support throughout the program.

1. INTRODUCTION

Electromigration is of major concern as a potential failure mechanism of VLSI metallization systems. Because of the small cross-section of the metal runs on VLSI circuits and the resulting high current density and potentially high chip temperature, electromigration can cause premature failure due either to voiding or line-to-line shorting. Electromigration has been controlled in LSI microcircuits by imposing an arbitrary limit on the design current density. While this approach has been satisfactory to date, its applicability to VLSI microcircuits is limited for two reasons. First, the present current density limit may not be tolerable since it limits the circuit density which can be achieved. If a metallization system is resistant to electromigration and can operate at current density above 2×10^5 A/cm^2 for long periods without failure, the designer should not be unnecessarily constrained. Secondly, the present limit may not be sufficiently low to preclude failure as the line width becomes smaller, unless an electromigration resistant metal system is used. In other words, the use of a single current density limit may either unnecessarily constrain the use of a resistant metal system or insufficiently constrain a non-resistant system, or both.

This report presents the results of an investigation of a new approach for assuring that a new VLSI metallization system is not susceptible to premature failure due to electromigration. A metallization test procedure is defined which may be used to demonstrate that a new metallization system is capable of sustained operation at any desired current density. Rather than set one current density limit for all metal systems, a microcircuit manufacturer can use any selected current density as long as it passes the test for that current density. The vendor must "qualify" his metallization system for the current density design limit he selects.

While many investigators have studied electromigration phenomena, each one has used his own test samples, test procedures, and failure criteria. Therefore, there is little commonality between test methods and it is difficult to quantitatively compare the results obtained by different people for different metal systems. Some investigators accelerate their testing by using very high temperatures, while others use lower temperatures and higher current densities. Each investigator uses his own test sample configuration. The failure criteria may vary from a modest change in line resistance to permanent catastrophic open circuit. The method itself, may involve an accelerated life test, or a technique which estimates lifetime by extrapolating resistance change data. Temperature ramp and current ramp procedures have also been proposed. If a metallization qualification test is to be used, then a standard test method must be selected which would be used for the purpose. This test method may be included in future versions of Mil-Std-883, "Test Methods for Microelectronics."

The objective of this study is to explore the feasibility of developing a standard metallization test method, to determine the approach to be used, and to develop a candidate test method description. Several aspects of the problem of creating a standard test method have been explored:

- The possibility of using a resistometric method, such as the TRACE, to evaluate useful electromigration life.

- The statistical distribution of times to failure was evaluated so that an approach for predicting early failures could be developed.

- The dependence of lifetime on line length was evaluated.

Based on these results, as well as the published results of other workers, a candidate test method was developed.

Section 2 contains a description of the test approaches which were considered on this program. Section 3 presents the results of some exploratory tests in which the resistance variation due to electromigration was studied in detail in order to assess the validity of resistometric methods for evaluating metallization lifetime. Section 4 describes a large scale life test program designed to explore failure statistics, line length dependence and the statistics of resistance variations. In Section 5 an approach to a standard test is presented and the rationale given. The Appendix contains a summary of the candidate test method.

2 TEST APPROACHES

Two test methods are typically used to obtain electromigration failure rate data. These methods are discussed below.

2.1 RESISTOMETRIC TECHNIQUES

The resistometric technique is based on measuring the change in resistance during electromigration for a specific set of accelerated conditions. A relationship is then derived relating failure as a function of change in resistance with time to temperature, and current density. Two of the possible resistometric techniques were considered for their use in this program, and are described here.

2.1.1 Temperature Ramp Resistance Analysis Technique (TRACE)

The TRACE method was developed at Syracuse University [1]. In this technique a sample is subjected to a fixed current density and the temperature is ramped up at a fixed rate. The resistance is monitored as a function of time and by a rather involved analysis of the resistance-time curve, an activation energy and pre-exponential constant for the resistance change mechanism is obtained. The developers of this technique claim that this test may be used to assess the susceptibility of a metallization system to electromigration in a relatively short time of a few hours using a small number of samples. As reported, the technique requires packaged samples.

2.1.2 Residual Resistance Techniques

It was known that the resistance of a metal line generally increases with time due to electromigration, eventually leading to failure due to an open circuit. It was also known that voids form in the line and that failure occurs when a void completely severs the line. Therefore, it is evident that void formation is responsible for much of the resistance increase, at least late in the life of the line. Early in the life of the line, before visible voids are seen, resistance changes may be due to vacancies and other defects introduced by the electromigration process, and the rate of resistance rise early in life may be indicative of the rate of occurrence of the basic electromigration mechanism. The TRACE technique described above involves an assessment of this early resistance change and the kinetic parameters it measures may represent those of the basic electromigration mechanisms.

Mattheissen's rule [3] states that the resistance of a metal line is given by the sum of a temperature independent component, R_O, and a temperature dependent component, R_T, or,

$$R = R_O + R_T \qquad (1)$$

where the temperature independent component is due to electron scattering from defects and impurities in the lattice, while the temperature dependent component is due to scattering by lattice phonons. The dependence of R_T on temperature is approximated by the Gruneisen relation [5],

$$R_T = R_o f(T/\theta) \approx \left(\frac{T}{\theta}\right)^5 \int_0^{\theta/T} \frac{x^5 e^x \, dx}{(e^x-1)^2} \qquad (2)$$

The constant θ is a characteristic temperature of each particular metal, and is close to the Debye characteristic temperature for specific heats. Figure 1 shows a curve plotted using points generated by numerical integration of the Gruneisen equation. The curve is normalized for aluminum with θ = 395°K. As can be seen from Figure 1, the curve approaches zero as temperature approaches absolute zero.

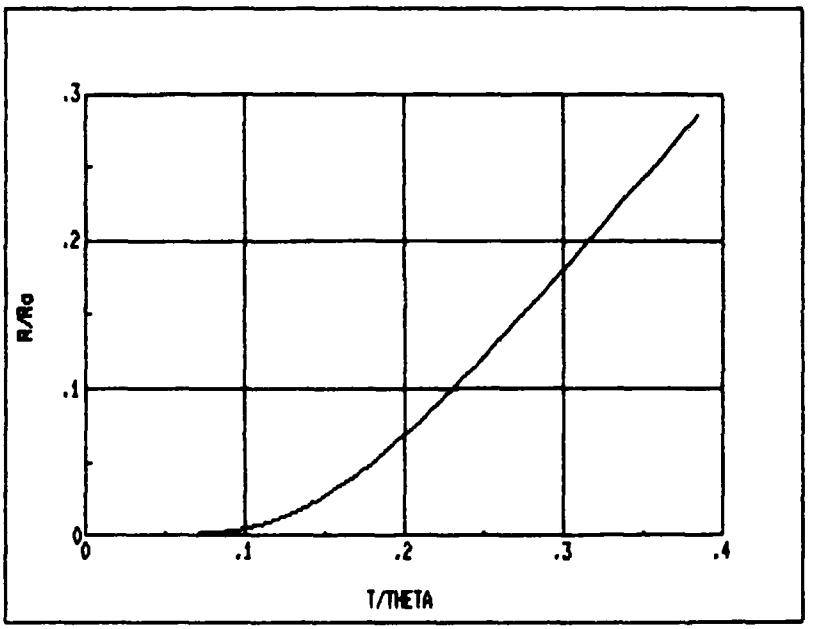


Figure 1. Temperature Variation of Resistance of Pure Aluminum with Theta = θ = 395°K

If the early resistance change is due to defect accumulation in the metal, R_o should change but R_T should not. If the resistance change is due to voiding which reduces the effective cross-section of the line, then R_T should change and not R_o. Assuming the former is true, a measurement of the resistance at a very low temperature where R_T is low would make it possible to detect very small changes in R_o and make it possible to characterize the electromigration kinetics very early in life. Likewise, it might be possible to evaluate electromigration at low levels of acceleration.

2.2 LIFE TESTS

The most common technique for evaluating the suceptibility of a metallization system to electromigration is accelerated life testing. This technique consists of subjecting a statistically significant sized group of samples to elevated temperatures and/or high current densities until failure occurs. The distribution of times to failure has been found to fit a log-normal distribution and therefore by plotting the failure time on log normal paper and fitting a straight line to the data an estimate can be obtained for the median-time-to-failure (t_{50}) and σ of the distribution. The (t_{50}) is used as a measure of the susceptibility of the line to electromigration under the applied stresses. An equation of the following form is used to relate values of t_{50} obtained under different stress conditions,

$$t_{50} = A\, j^{-n} \exp(\varepsilon / kT) \qquad (3)$$

where

A = a constant (independent of T or j)

j = the current density

n = a parameter which is approximately 1.5 - 2.0

ε = the activation energy (0.5 - 0.8 e.v. for aluminum)

and

k = Boltzmann's constant.

Often life tests are carried out at several temperatures and current densities and the resulting values of t_{50} are substituted into Equation (3) and the parameters n and ε determined. An estimated t_{50} at use conditions may then be obtained.

This life test technique can be done at the wafer lever using a controlled temperature heated chuck and electrical probes [2], or using packaged samples, test racks, and an oven.

3 EXPLORATORY TESTS

Early in the program a series of tests were done to learn more about change in resistance which occurs during electromigration so that the resistometric and residual resistance techniques for life prediction could be assessed.

Electromigration test samples fabricated several years ago were available for testing early in the program. The circuit, the tests performed, and test results are described in the following sections.

3.1 TEST PATTERN

Figure 2 shows a diagram of one-half the test pattern. Each individual electromigration test stripe has Kelvin contacts and parallel metal stripes on each side to test for lateral extrusion. Each of the four (4) test locations contained six (6) electrical connections, and it was therefore convenient to mount the sample die in 24-lead ceramic DIP packages. Figure 3 shows a sample die wire bonded in a 24 pin package. A description of the sample fabrication details is given in Table 1.

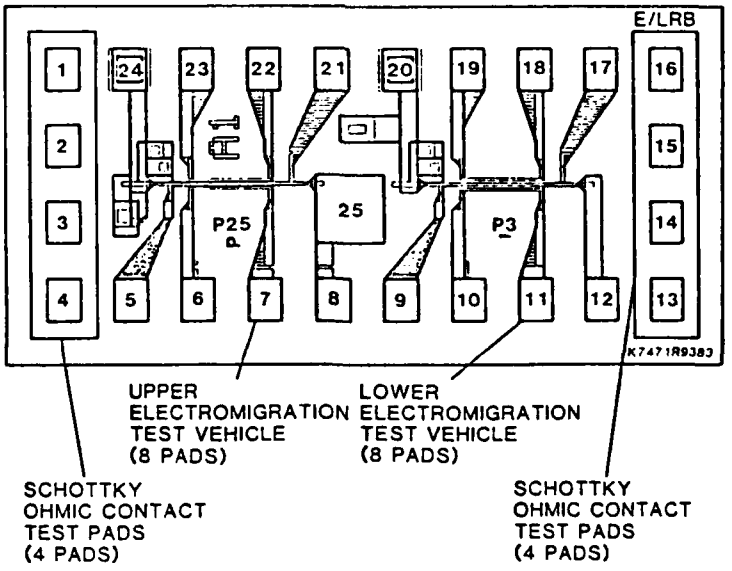


Figure 2. Electromigration Test Pattern

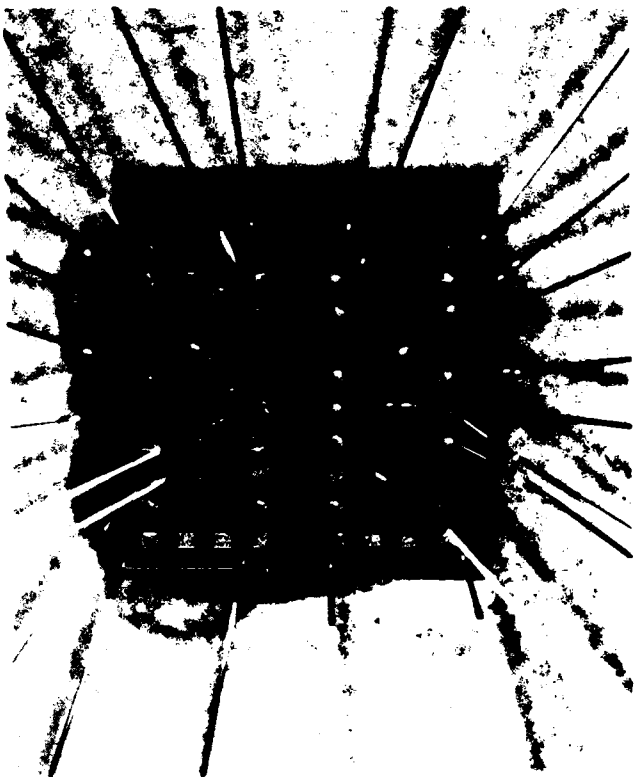


Figure 3. Electromigration Test Sample Die Wire Bonded in 24 Pin Dip

TABLE 1. ELECTROMIGRATION TEST SAMPLE DESCRIPTION

Metal Deposition Technique	E-beam Evaporation
Metal Thickness	1.6 μm
Oxide Thickness	0.4 and 0.8 μm
Composition	Al-2% Si
Overcoating	SiO_2
Line Width	7 μm
Line Length	1000 μm
Metal Anneal	1 Hr. 500°C, Forming Gas

3.2 RESIDUAL RESISTANCE TESTS

The validity of the theory concerning residual resistance and lifetime, as discussed in Section 2.1.1, was evaluated early in the program. Samples were selected and resistance as a function of temperature was characterized from liquid nitrogen temperature (77°K) to 573°C. Figure 4 shows a typical graph of resistance versus temperature over this range. This graph was generated by passing a low constant current (1 ma) through the sample stripe and measuring the resultant voltage at Kelvin contacts.

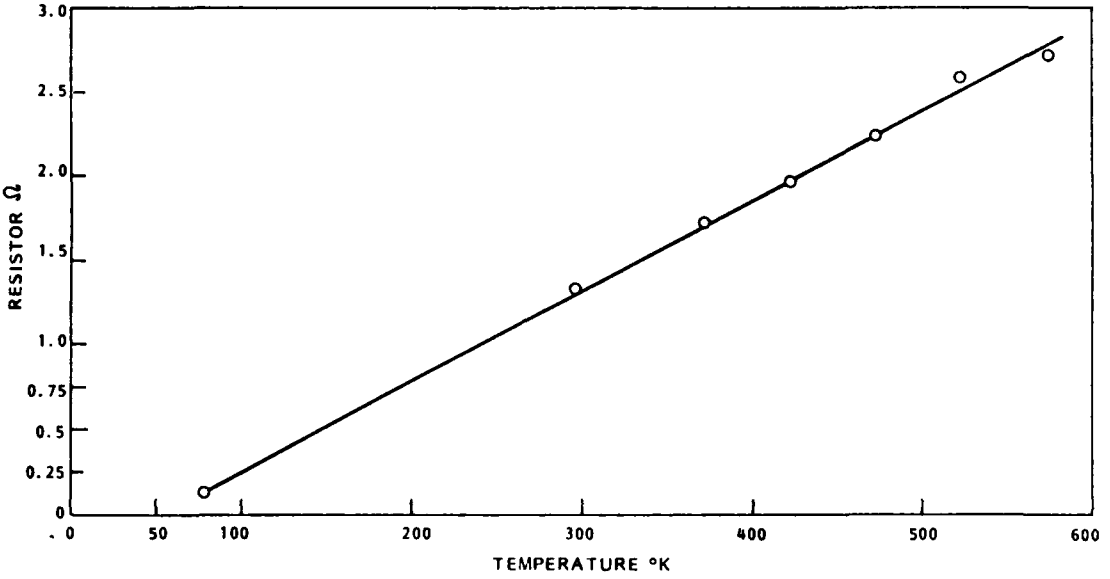


Figure 4. Resistance versus Temperature Sample 2, Line A3-1

A set of electromigration test conditions which would provide rapid results were selected. The equation from Section 2.2 was used to estimate a typical lifetime based on the set of conditions selected. An approximate value of the constant A was calculated from failure data found in reference [2]. The t_{50} equation was evaluated using the following:

$A = 3.1 \times 10^{8}$

$J = 3 \times 10^{6}$ A/cm^2

$n = 2$

$E_a = 0.5$ eV

$K = 8.61 \times 1^{-5}$ eV/°K

$T = 433$°K (160°C)

with these values:

$t_{50} \sim$ 23 hours.

This was judged to be a reasonable length of test time, and the temperature of 160°C and current density of 3×10^6 A/cm^2 were adopted as test conditions.

Samples were tested and measured according to the following plan:

- Measure resistance at 77°K and 25°C
- Stress at accelerated conditions approximately 1-2 hours
- Measure resistance at 77°K and 25°C
- Continue cycles until failure.

Results from testing sample 2, A3-1 will be discussed here.

Figure 5 is a graph of increase in low temperature resistance after 12.5 hours of electromigration. Figure 6 shows the increase in total resistance for the sample over the 12.5 hour test time. While the resistance measured at 77°K did increase, the increase at 25°C was much larger. This implies that even early in life the resistance change is due primarily to voiding, not defect accumulation. Therefore, the residual resistance technique was shown to be invalid and was not pursued further.

3.3 RESISTANCE VERSUS TIME EXPERIMENTS

During the tests described above it was noticed that during some of the period of electromigration the voltage being monitored at the Kelvin contacts was varying by significant amounts. This phenomenon was investigated during further testing by monitoring the Kelvin contact voltage with a strip chart recorder while electromigration was taking place. It was verified that the sample stripe resistance was indeed rapidly fluctuating by 50% or more during electromigration testing.

A method was devised to carefully study the R(t) function in detail. The test set-up is shown in Figure 7. A fixed constant current was established through the line while the voltage drop across the Kelvin contacts was monitored by both a digital voltimeter (DVM) and a dual trace chart recorder. The recorder was set on one of two sensitivities, differing by a factor of 100. When operated on the more sensitive scale, it was necessary to apply a "bucking" voltage in series with the recorder in order to keep the recorder on scale. A highly regulated variable voltage source was used for this purpose. The temperature of the sample was monitored by a thermocouple placed under the center of the DIP between the package and the test socket.

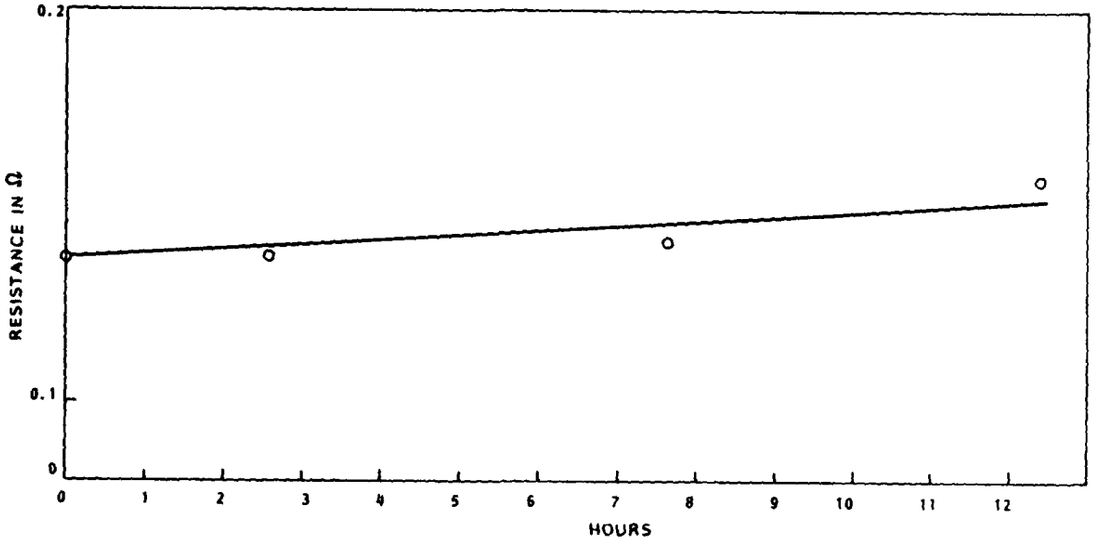


Figure 5. Increase in Residual Resistance after 12.5 Hours of Electromigration. Sample 2, A3-1

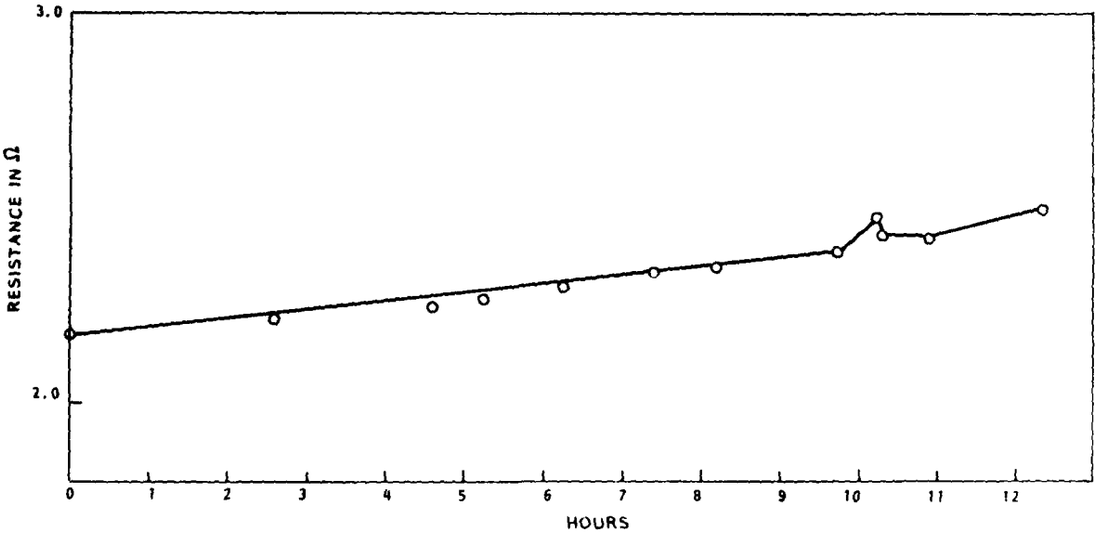


Figure 6. Increase in Total Resistance After 12.5 Hours Electromigration Sample 2, A3-1

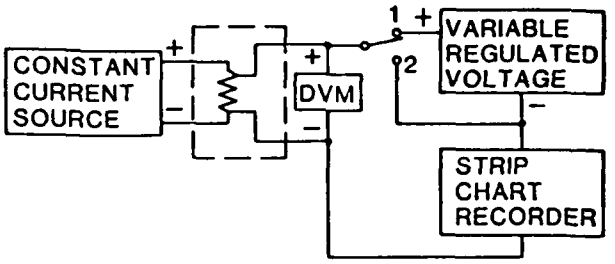


Figure 7. Resistance Monitoring Circuit

Several sample die were cross-sectioned for optical and SEM examination to determine average test stripe metallization thickness. Optical measurements were used to determine average stripe width. These measurements were used to calculate stripe cross-sectional area, and the constant current necessary to maintain current density of $\sim 3 \times 10^6$ A/cm^2 was calculated. In order to keep the current density at the same value in all the tests performed, the current was adjusted at the beginning of each electromigration test so that 427 mV were measured at the Kelvin contacts. This was the voltage produced at the Kelvin contacts of the first sample tested, and was thereafter adopted as the standard.

Adjusting the current at the beginning of each test so that a specific voltage was produced serves to remove the effect of any cross sectional variations that might occur from sample to sample. This is true because of the following relationship:

$$V = RI = \rho \frac{\ell}{A} I = \rho \frac{\ell}{A} J A = \rho \ell j \qquad (4)$$

$$j = \frac{V}{\rho \ell}$$

where: V = Voltage

R = Resistance

I = Current

ρ = Resistivity

ℓ = Sample Length

Δ = Cross Sectional Area

j = Current Density

Therefore, assuming that sample length (ℓ) and metal resistivity (ρ) do not change significantly from sample to sample, current density can be kept the same by beginning with the same voltage for each test performed. Sixteen (16) samples were tested to failure using the apparatus shown in Figure 7 and the following conditions:

Temperature = 160°C

Current Density $\simeq 3 \times 10^6$ A/cm^2

Initial Voltage = 427 mV

Figure 8 contains reproductions of selected resistance vs. time charts. These charts were selected to illustrate both the common features and the variations found from sample to sample. All of the samples exhibit an early, almost linear rise in resistance for the first 2-3% change. The rate of rise was very similar for most samples and was not correlated with ultimate life. The behavior shown in the charts after the initial rise varies greatly from sample to sample with the following observations:

- Short term spikes of varying amplitude occur, which may represent short term open circuits. These can occur relatively early in the life of the line (life is defined as a permanent open circuit).
- The spikes appear to occur randomly in time and amplitude.
- Both positive and negative steps occur, again randomly.
- A line may "fail" many times and heal before the final permanent failure.
- The ultimate life appears to depend more on the ability of the line to heal (a reduction in resistance) than in the rate of rise of resistance.

Figure 9 is a reproduction of a chart obtained with the recorder set on the most sensitive scale (10 mV full scale) during the first 5 hours of life, during the nominally linear portion of the curve. It is obvious that the rate of rise in resistance is not constant or linear, but also includes spiking and positive and negative steps on a much smaller scale than those seen in Figure 8. Therefore, the erratic behavior occurs very early in the life of the line with the variations appearing to grow in amplitude with time. Fluctuations as small as 0.1 mV (0.2%) are observed.

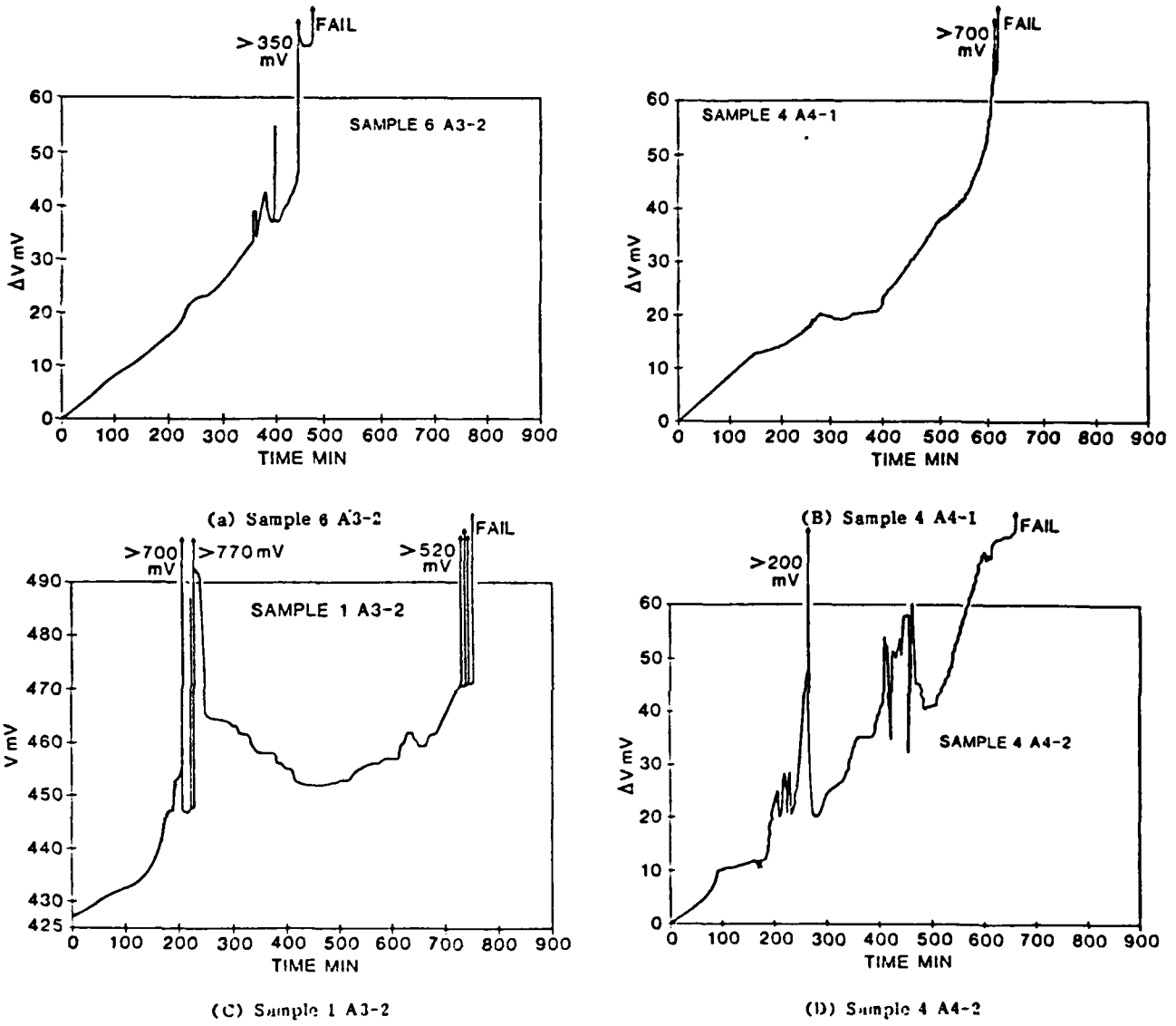


Figure 8. Resistance versus Time Charts

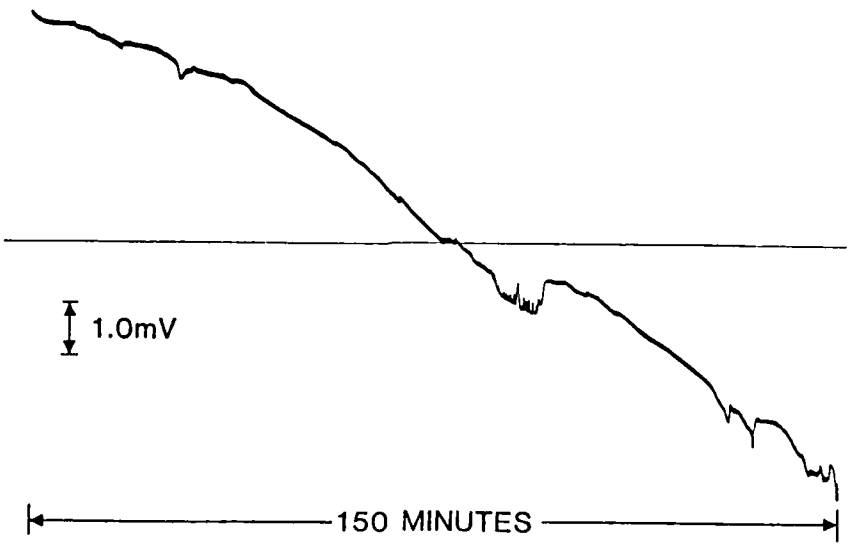


Figure 9. Voltage Drop vs Time on Most Sensitive Scale During Early Life

3.4 VOID OBSERVATIONS

An experiment was conducted to attempt to relate the resistance variations to the development and growth of voids in the line. The glass was removed from a line so that voiding would be visible in the Scanning Electron Microscope (SEM). The line was subjected to 160°C, 3×10^6 A/cm^2 stress which was interrupted periodically so that the line could be examined in the SEM. Figure 10 displays a sequence of SEM photographs of the line taken during the life of the line. The number and size of the voids increase with time with many large voids having accumulated by the end of 590 minutes.

Figure 11 shows the increase in resistance as a function of time for the line, measured at the times the SEM photos were taken. Also plotted are the number of voids, #, and the transverse length of voids, ℓ_T, obtained from the SEM photographs. The "total transverse length" is the sum of the void lengths measured perpendicular to the direction of the line. The resistance increases almost linearly in this sample while the number of voids increases rapidly at early time followed by a linear increase which parallels the resistance curve. The number of voids saturates at later times as small voids merge to form larger voids. The total transverse void length increases linearly in parallel with the resistance curve after a rapid initial increase.

Figure 10. SEM Photographs of Test Line during Electromigration

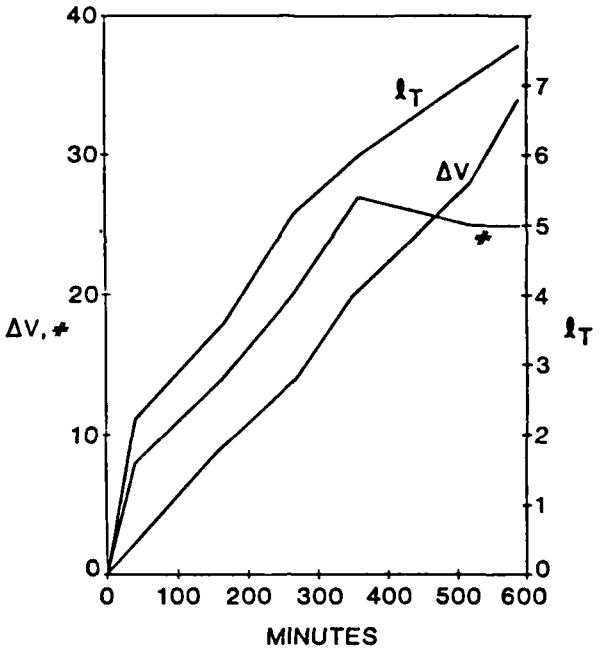


Figure 11. Void Characteristics versus Voltage Variation

These results indicate that for the line studied, the resistance change during life occurs coincidentally with the formation and growth of voids even at relatively early times. These results are consistent with the results of the residual resistance experiments which also indicated that resistance change is due primarily to voiding, even early in life.

3.5 RESISTANCE MODELING

The causes of the resistance variations with time shown in Figures 8 and 9 are not clear. Since the increase in resistance is apparently associated with the formation and growth of voids in the line, as indicated by Figure 11, in order to understand these variations it is important to understand the effects of voids on the measured voltage drop across a thin film metal line.

A finite element analysis of a voided line was carried out using the ANSYS* finite element program. This general purpose computer aid includes a 3-D thermal-electrical solid element which provides both a thermal analysis

* Swanson Analysis Systems Inc., Houston, PA.

and an electrical analysis for a conductor with a defined geometry under a defined electrical stress. Using this element, both the local electric field and temperature can be calculated for a given stripe geometry and thermal boundary conditions. The geometry used in the modeling is shown in Figure 12. The width, metal thickness, and oxide thickness are approximately those of the sample lines. The silicon substrate temperature is assumed to be 160°C with an initial current density of 3×10^6 A/cm^2, also the stresses used in the tests reported above. Calculations were done for four cases:

- No crack
- Crack length = 50% line width
  Crack depth = 80% line thickness
- Crack length = 90% line width
- Crack depth = 80% line thickness
- Crack length = 90% line width
- Crack depth = 100% line thickness

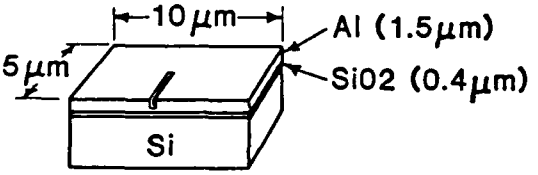


Figure 12. ANSYS Model of Void

The results of the analysis are summarized in Table 2. The results for Case 1 agree closely with the measured results for the sample lines, both in measured voltage drop and in the extent of self-heating. The results for this case indicates that the temperature gradient in the aluminum and in the silicon is very small with nearly all of the temperature drop occurring across the oxide layer. Therefore, the amount of self-heating is very sensitive to the oxide thickness and insensitive to the metal thickness.

TABLE 2. ANSYS FINITE ELEMENT ANALYSIS RESULTS

CASE	CRACK DEPTH (μm)	CRACK LENGTH (μm)	TEMPERATURE MAX.	Δ	VOLTAGE DROP (V)
1	0	0	182°C	22°C	.0168
2	1.2	2.5	185°C	25°C	.0185
3	1.2	4.5	189°C	29°C	.0209
4	1.5	4.5	227°C	67°C	.0441

A small void which does not penetrate through the thickness of the line (Case 2) causes a relatively minor increase in voltage drop (1-2 mV) and a small increase in temperature (3°). Since the variations in voltage drop shown in Figure 9 are as small as 0.1 mV, it is clear that our experimental measurements are sensitive to the growth and behavior of very small voids. The formation or annihilation of individual small voids could result in resistance fluctuations of the magnitude shown in Figure 9.

Extending the crack of the same depth to 90% of the way across the line (Case 3) results in another small temperature increase and another 2.4 mV increase in voltage drop. However, if the crack penetrates all of the way through the thickness of the line (Case 4), the maximum temperature rises 38°C and the voltage drop increases by 25.6 mV. Therefore, a void which suddenly penetrates completely through the metal thickness will cause a rapid and large increase in voltage drop. This may explain some of the positive steps seen in the resistance-time curves.

While the temperature of the line increases appreciably for Case 4, the temperature rise is small compared to that necessary to melt open the lines. Since the cross-sectional area of the line for this case has been reduced to 10% of the original area, it is clear that the void would have to reduce the area to much less than 10% of the starting value in order for melting to occur. Therefore, melting will be a factor only for lines which are almost completely severed by voiding. For lines on thicker oxide layers this area reduction necessary for melting will be smaller.

Figure 13 is a contour plot generated by the ANSYS program for the Case No. 4 showing the temperature distribution near the void. As expected, the line is hottest at the end of the void. While this spot is 67°C above the substrate, the temperature in the line segment varies by only 20°C. The thermal conductivity of the metal is high enough that the thermal effect of the void extends well beyond the 10 μm segment shown in the figure. This implies that two voids within 10-20 μm of each other can interact thermally. The total temperature rise due to a cluster of voids may be much higher than that of an individual void, making melting and catastrophic failure more probable.

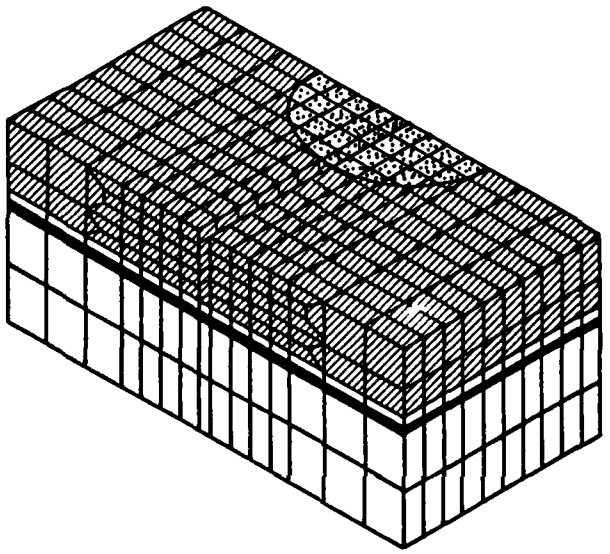


Figure 13. ANSYS Temperature Contours, Case 4

Figure 14 is a similar contour plot showing the distribution of potential across the same line segment. The potential gradient is greatest near the open end of the void. Of particular interest is the fact that the potential difference across the open end of the void is 35 mV. For narrow voids, the electric field across the top of the void can be very high. 3.5×10^5 V/m cross a 1000 Å wide void. This raises the possibility of electrical discharges being developed across narrow voids, even before the lines are completely severed by the void. If the metal is covered by a glass or nitride layer so that the atmosphere in the void is at a reduced pressure, these discharges could occur at lower electric fields making their occurrences more probable. Such a mechanism may explain some of the "healing" phenomena observed in the resistance-time curves.

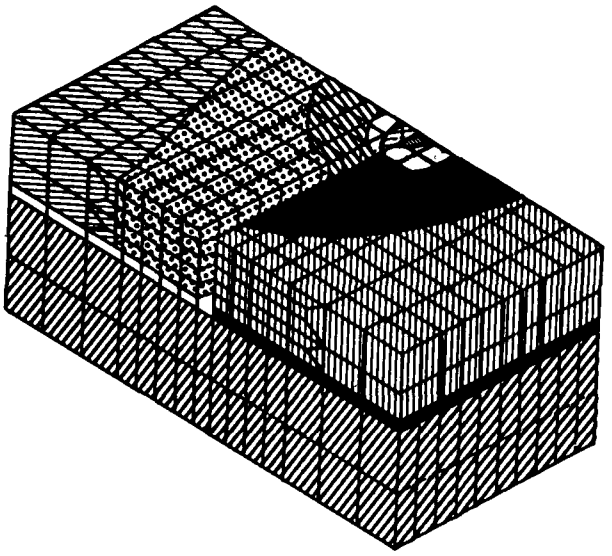


Figure 14. ANSYS Voltage Contours, Case 4

3.6 INTERIM DISCUSSION

The resistance time measurements reported in Section 3.3 demonstrated that the resistance variations during electromigration can be quite complex, even at the earliest times. Sudden increases and decreases in resistance occur and the stripe can open and then heal many times before final failure. It is clear that the degradation of a stripe involves multiple mechanisms, all of which together define the ultimate life of a specific stripe.

The overall resistance increase appears to be primarily due to the formation and growth of voids. Sudden increases in resistance may be associated with the penetration of voids to the bottom of the stripe. Decreases in resistance may be associated with the ignition of discharges across partial voids. It is also possible that narrow voids may grow across the stripe causing the temperature in the vicinity of the void to increase. This increase may cause an expansion of the metal which causes the void to close, resulting in a relaxation oscillation, which may explain some of the cyclical variations observed in the resistance-time curves. Levine and Kitcher [6] have reported observing the movement of voids down the stripe, eventually moving into the bonding pads. Such behavior would also be consistent with the complex behavior of the resistance with time.

It is clear that the ultimate failure of a stripe does not occur as a result of a single process in which a single void grows until the stripe is severed. The ultimate failure time is determined not only by the growth rate of voids but by their dynamics; by their interaction with other voids and with the thermal and electrical perturbations caused by the voids themselves. It should not be expected that the stripe lifetime is correlated with the initial rate of rise of resistance since this early increase may be determined only by the rate of void formation early in the process and does not measure the effects of all of the other mechanisms which determine stripe lifetime. Likewise, it is not clear that the activation energy determined by a conventional life test approach will be the same as that measured using resistometric techniques since the ultimate lifetime is determined by several different mechanisms, which may have different activation energies, while the resistometric techniques measure the effects of only those mechanisms which affect the resistance early in life.

Therefore, based on these preliminary experiments and modeling it was tentatively concluded that resistometric techniques are not suitable for determining the susceptibility of a metallization system to failure due to electromigration and that tests to failure (life tests) would be required for this purpose.

4 LARGE SCALE LIFE TESTS

4.1 OBJECTIVES

A large scale electromigration life test was carried out with several objectives:

- To verify statistically the tentative conclusion that resistance change early in life is not correlated with time-to-failure and, therefore, that resistometric techniques alone are not suitable as a standard test procedure.

- To study the distribution of time-to-failure for a large sample size to determine whether it is log-normal. For the purpose of a qualification test, the time-to-first-failure is more important than the median-time-to-failure. In this study, the time-to-first-failure has been approximated by the time for 0.1% of the samples to fail ($t_{0.1}$). In order to determine $t_{0.1}$ it will either be necessary to test 1000 or more samples, or to test a smaller number of samples and extrapolate the measured distribution curve down to the 0.1% point. In order to do this extrapolation with confidence it is necessary that we know the form of the distribution and be sure that it is valid down to the 0.1% point. Since most life tests reported in the literature involve at most a few tens of samples, the range over which the log normal distribution has been verified is not adequate. In fact, over a narrow range, a logarithmic extreme value or even a normal distribution may often be equally valid.

- To study the dependence of the failure statistics on line length. Several studies have shown that the t_{50} and σ both decrease as line length increases. Agarwala et al [7] found that t_{50} decreased rapidly as length increased below about 200 μ but that for larger lengths it changed little. Attardo, Rutledge, and Jack [8] subsequently showed that this behavior is predictable by a simulation procedure. Shoen [9] used a Monte Carlo simulation procedure to show that the forms of the length dependence of t_{50} and σ are:

$$t_{50} \propto \exp(\beta/L) \tag{5}$$

and

$$\sigma \propto \gamma L^{-\delta} \tag{6}$$

where β, γ, and δ are positive constants. Little data is available comparing lines with widely varying line length. This data is needed to confirm the simulation results so that an optimum line length may be selected for a standard test procedure.

4.2 TEST CIRCUIT

An electromigration test circuit was designed for use in the large scale life test. The circuit is shown diagramatically in Figure 15, and Figure 16 shows a wire bonded unit in a 24 pin DIP package. Because of test fixturing, the 24 pin DIP packaging format was retained for the life test. The life test circuit utilizes two (2) parallel lines alongside each of the four (4) test stripes to monitor for lateral metal extrusion. The circuit is described in Table 3.

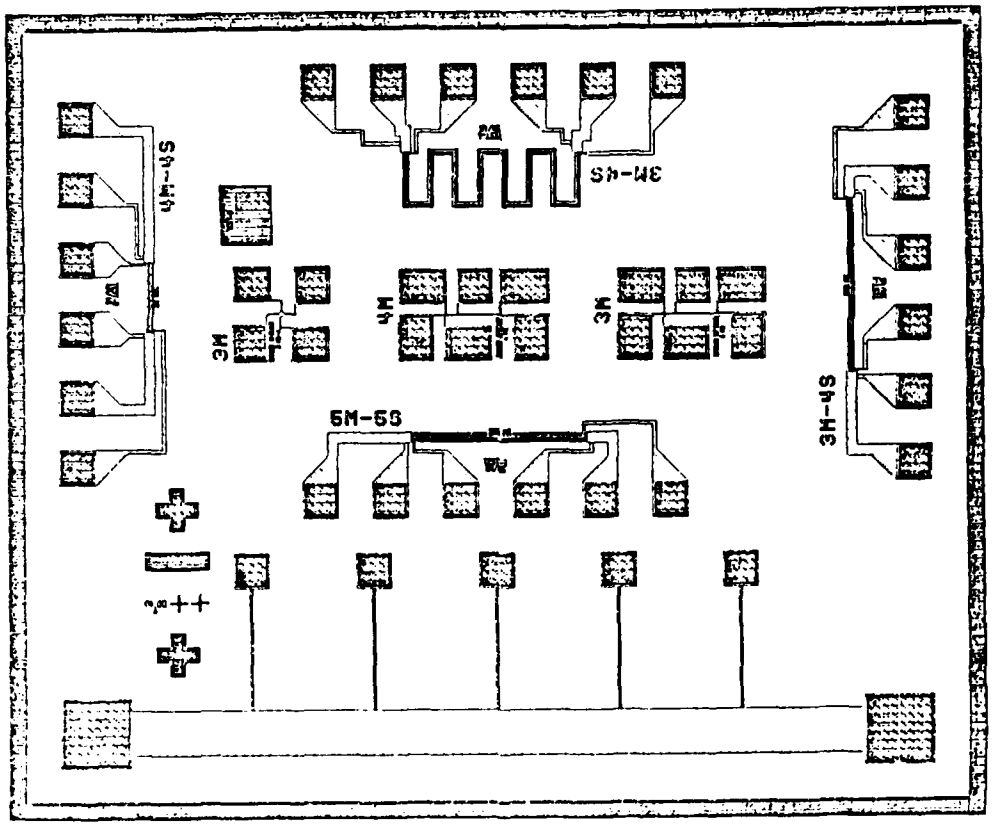


Figure 15. Electromigration Test Pattern

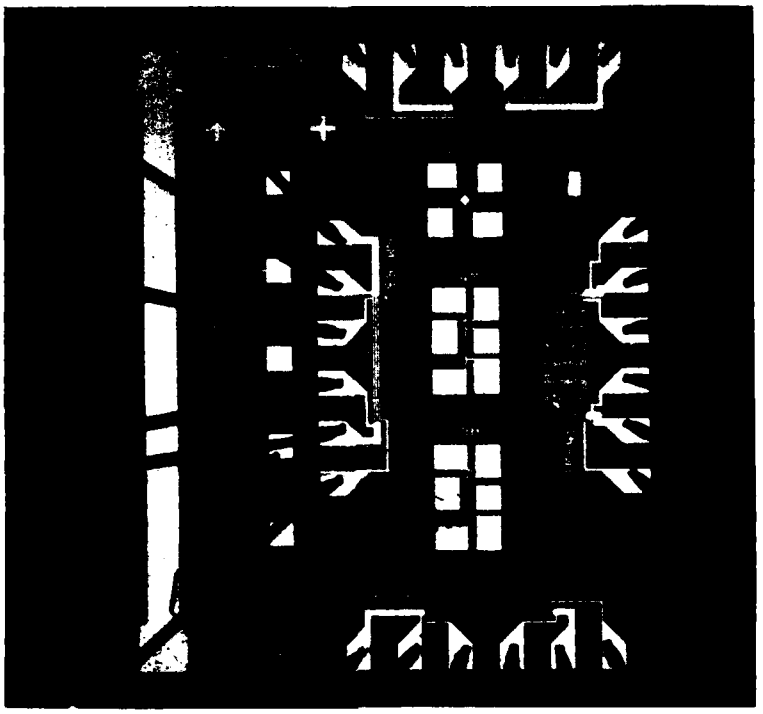


Figure 16. Electromigration Test Sample Wire Bonded in a 24-Pin DIP Package

TABLE 3. DESCRIPTION OF ELECTROMIGRATION TEST CIRCUIT

	PROCESS
Metal Deposition	Sputtered
Metal Thickness (μm)	0.8
Oxide Thickness (μm)	0.4
Composition	Al + 1% Si
Overcoat	SiO_2
Overcoat Thickness (μm)	0.4
Anneal	1 Hour 400°C, Hydrogen

LINES

Number	Length (μm)	Width (μm)
1	500	4.5
2	500	5
3	200	3.4
4	1650	3.4

4.3 PRELIMINARY TESTS

Several samples of line 4 (3.4 μm wide, 1650 μm long) were tested individually using the apparatus and conditions described in Section 3.3. These samples exhibited the same type of resistance versus time behavior as described in Section 3.3, but to a much lesser degree. As Figure 17 shows, small positive and negative changes in resistance occur as electromigration takes place. As in the earlier tests, these changes begin almost immediately and become much larger toward the end of life.

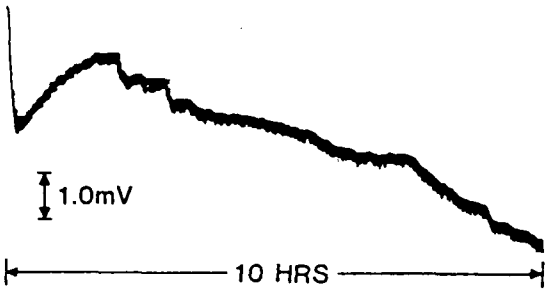
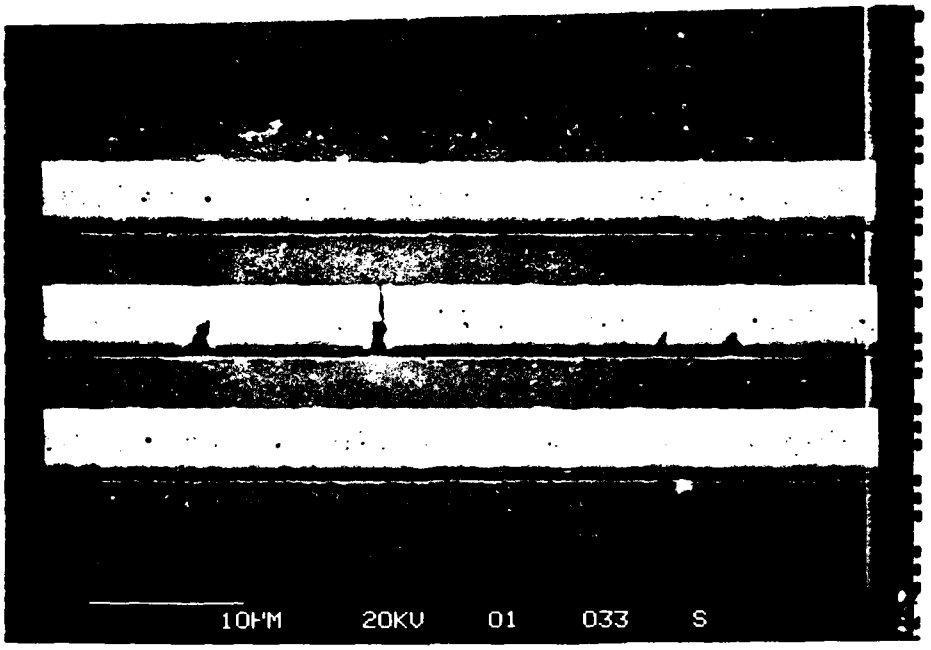
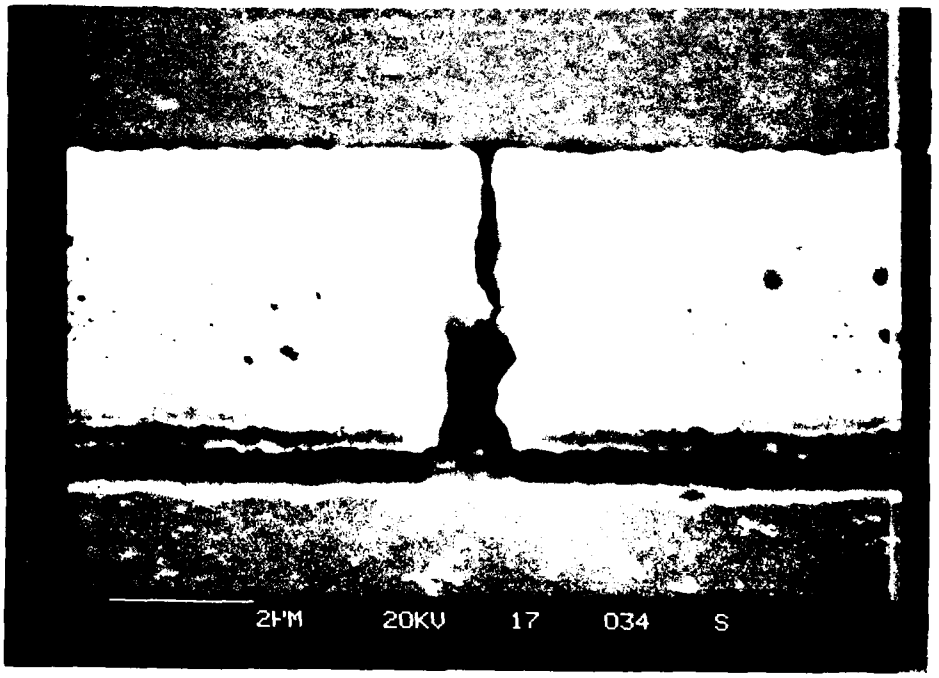


Figure 17. Voltage Drop vs Time for Electromigration Samples

Optical and SEM examination of failed units showed that only a few voids were formed during electromigration, with final catastrophic failure occurring at the largest void. Figures 18 and 19 show typical voids formed during electromigration using these samples with sputtered aluminum-silicon metallization. Figure 18 shows failure of a type 2 line, 5 μm wide and 500 μm in length. Figure 19 shows failure in a type 4 line, 3.4 μm wide and 1650 μm long. In both cases, failure occurred at the largest void in the line. Comparison of Figures 18 and 19 with Figure 10 clearly demonstrates the difference in number and type of void formation in the metallizations of the two types of samples evaluated in this program.

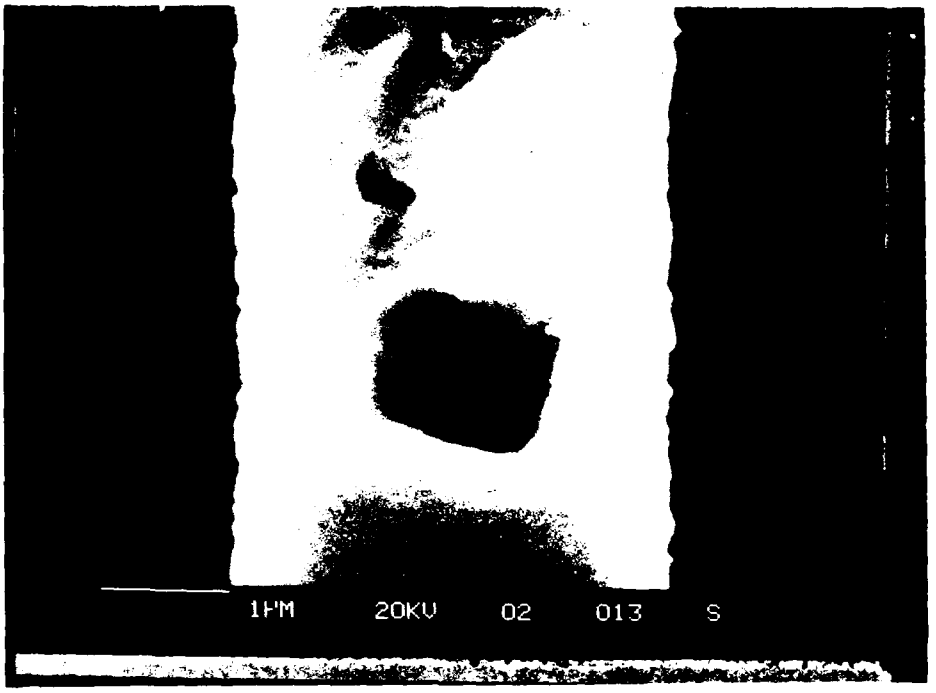


a. Overall View of Voids

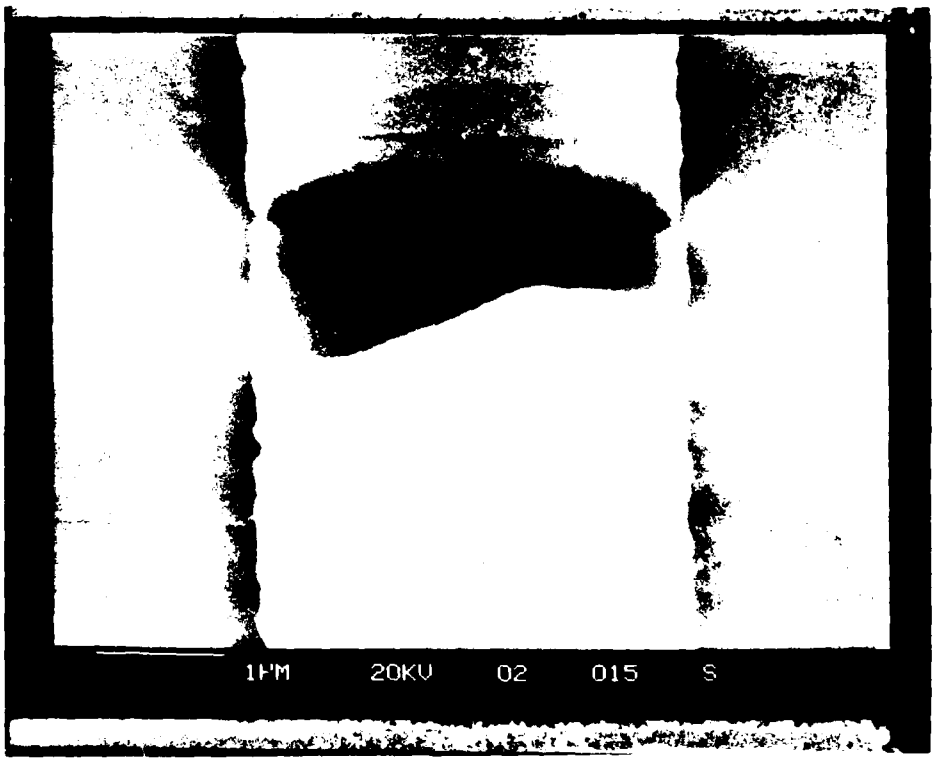


b. Large Void Where Failure Occurred

Figure 18. Typical Voids Produced in Type 2 Line, 5 μm Wide, 500 μm Long



a. Void Occurring in Center of Test Stripe



b. Large Void Where Failure Occurred

Figure 19. Typical Voids Produced in Type 4 Line, 3.4 μm Wide, 1650 μm Long

4.4 LIFE TEST APPARATUS

Apparatus for simultaneously life testing 300 metal stripes at accelerated conditions was designed and constructed. Table 4 shows the breakdown of the 300 lines.

TABLE 4. ELECTROMIGRATION LIFE TEST

Boards	Units per Board	Lines per Unit	Total Number Lines
25	3	1 - 4.5 μm×500 μm	75
		1 - 5 μm×500 μm	75
		1 - 3.4 μm×200 μm	75
		1 - 3.4 μm×1650 μm	75

Figure 20 diagramatically shows the life test set up.

The test rack backplane was wired so that each of the four (4) groups of 75 test stripes was electrically connected in series with a constant current source. A reverse biased 3.0 volt zener diode was shunted across each test stripe. The function of this diode was to go into zener breakdown when the test strip failed open, preventing an individual stripe failure from stopping the life test.

A program was written for the HP-85 computer which controlled operation of the Datalogger. The Datalogger continuously scanned each of the 300 test stripes serially, measuring the voltage at the stripe Kelvin contacts. When all 300 voltage measurements were being made, the total scan time was approximately 30 seconds.

At the beginning of the test, a scan file was created and stored on tape. This scan file consisted of the following information on each of the 300 test stripes:

- Unit and stripe designation
- Time of day
- Date
- Total time under test
- Voltage at Kelvin contacts.

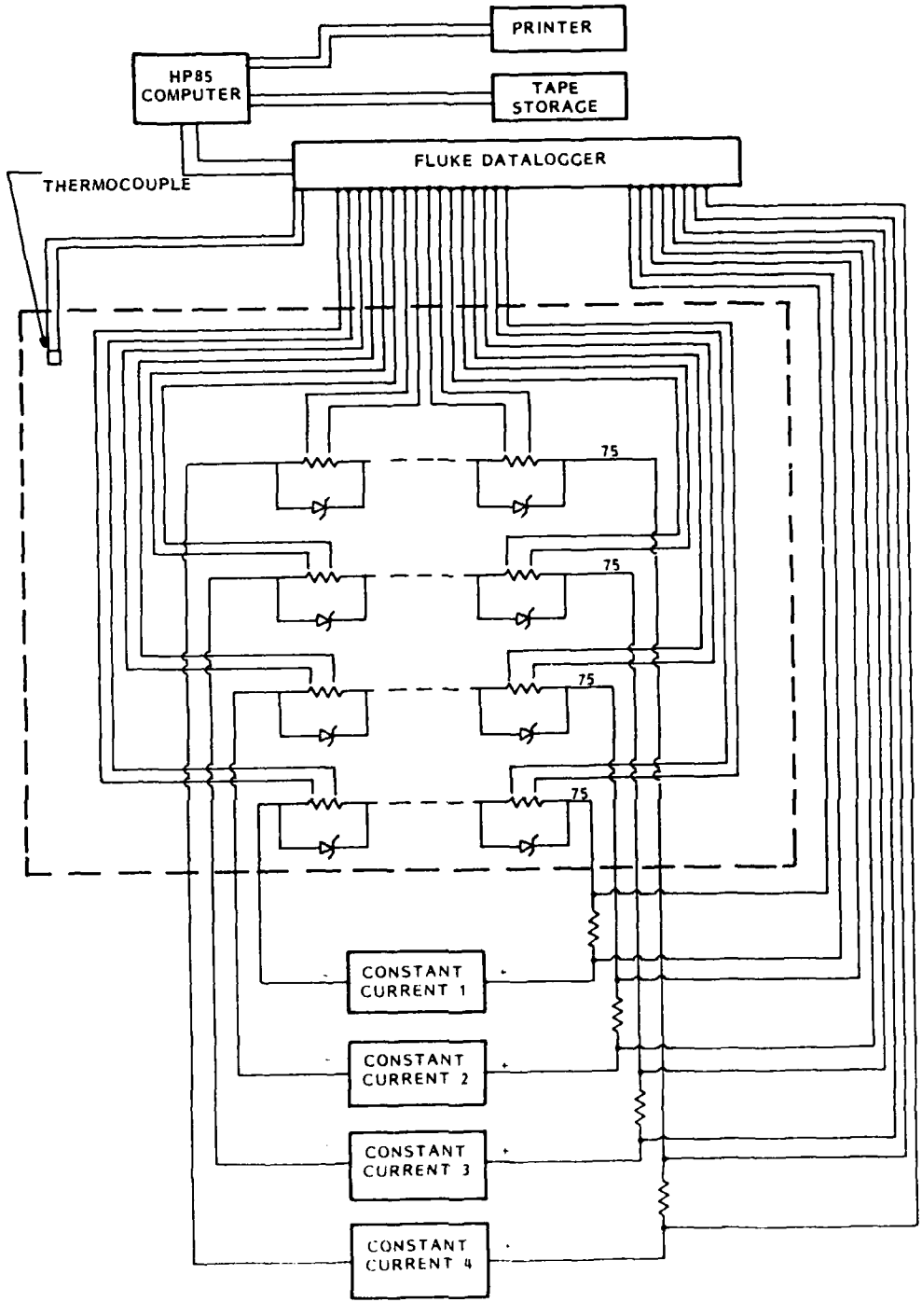


Figure 20. Life Test Setup for Simultaneous Test of 300 Lines

The initial voltage across each sample was stored in an array in computer memory. During each scan the new value for each line was compared to the value stored for that line in the array. The computer program was written such that a change in voltage of 1% would cause the information described above to be stored in a buffer for later storage on tape. Each time a change in voltage of 1% was recorded for a particular line, the new voltage was inserted into the array and became the base value against which succeeding voltage measurements were compared. Catastrophic failure was detected when the zener voltage was measured. In this way, complete resistance versus time information was recorded from beginning to end of life.

In addition to the serial voltage scan, the Datalogger was programmed to scan oven temperature in three (3) locations and to scan current values for the four (4) current supplies. If the temperature changed by ± 3°C or the current changed by ± 3%, the following information was recorded:

TEMPERATURE	CURRENT
• Thermocouple number	• Current supply number
• Time of day	• Time of day
• Date	• Date
• Total time under test	• Total time under test
• Temperature	• Current

A complete scan of all information was made every one (1) or two (2) days throughout the duration of the test. Both the scan files containing change in voltage and total sample scan were loaded into a VAX computer system for data analysis. The results of this analysis are discussed in a later section of this report.

4.5 LIFE TEST CONDITIONS

Because of two constraints, the set of test conditions used during earlier, preliminary tests (160°C, 3×10^6 A/cm^2) could not be used for the life test. The two constraints placed on the life test conditions were:

- Test boards limited to 150°C
- Voltage across test stripe 4 (3 μm × 1650 μm) was ~2.5 volts at current density of 3×10^6 A/cm^2 and T = 150°C.

The leakage current of the 3.0 volt zener diodes began to become significant at ~2.8 volts. It was felt that a larger safety margin would be needed to prevent zener leakage current from interfering with the life test.

The conditions selected for the life test were:

- Temperature - 150°C
- Current Density - 2×10^6 A/cm^2

4.6 TEST STRIPE SELF HEATING

When a high current density is set up in a thin film conductor, joule heating causes the conductor to rise above ambient temperature. This rise above ambient results in an additional acceleration factor that must be taken into account when analyzing life test results.

The self heating created during the life test was calculated for each of the four (4) test structures used. As Figure 4 in Section 3.2 shows, resistance is a linear function of temperature over the temperature range used during the life test.

Self-heating was calculated using the following steps:

- At room temperature, pass a low current (1 ma) through the stripes and measure voltage at Kelvin contacts
- At test temperature (150°C), pass a low current (1 ma) through the stripes and measure voltage at Kelvin contacts
- At test temperature (150°C), establish high current density (2×10^6 A/cm^2) and measure voltage at Kelvin contacts after stabilization period (~10 minutes).

The following relationship used the voltage and current data generated by the steps above to calculate self-heating.

$$(T_3 - T_2) = \text{Temperature Rise} = \Delta T = \left[\frac{\frac{I_1}{I_2} \cdot V_3 - V_2}{V_2 - V_1} \right] \qquad (7)$$

where

T_1 = Room Temperature

I_1 = Low Current (1 ma)

V_1 = Kelvin Contact Voltage at T_1 and I_1

T_2 = Life Test Temperature (150°C)

V_2 = Kelvin Contact Voltage at T_2 and I_1

T_3 = Temperature After Self Heating Stabilizes

I_2 = High Current Establishing 2×10^6 A/cm^2

V_3 = Kelvin Contact Voltage at T_3 and I_2

The self-heating was calculated for several samples using this technique, and all calculations agreed within a few tenths of a degree Centigrade. Table 5 gives the results of the self-heating calculations.

TABLE 5. CALCULATED SELF-HEATING OF TEST LINES

Line Number	Line Dimensions	Temperature Rise
1	4.5 μm × 500 μm	13°C
2	5 μm × 500 μm	14°C
3	3.4 μm × 200 μm	11°C
4	3.4 μm × 1650 μm	15°C

4.7 RESULTS

Two life test sequences were run involving a total of 600 lines, 155 lines of each type. Figures 21 and 24 present the resulting distribution of time-to-failure for the four types of lines plotted on log normal paper. Figures 25-28 are the results obtained for the second test and Figures 29-32 are the distributions using the combined data from the two tests. The tests were continued until nearly all of the type 1, 2, and 4 lines had failed. Because the type 3 lines had a much longer life, the tests were continued only until 50-60% of the lines had failed.

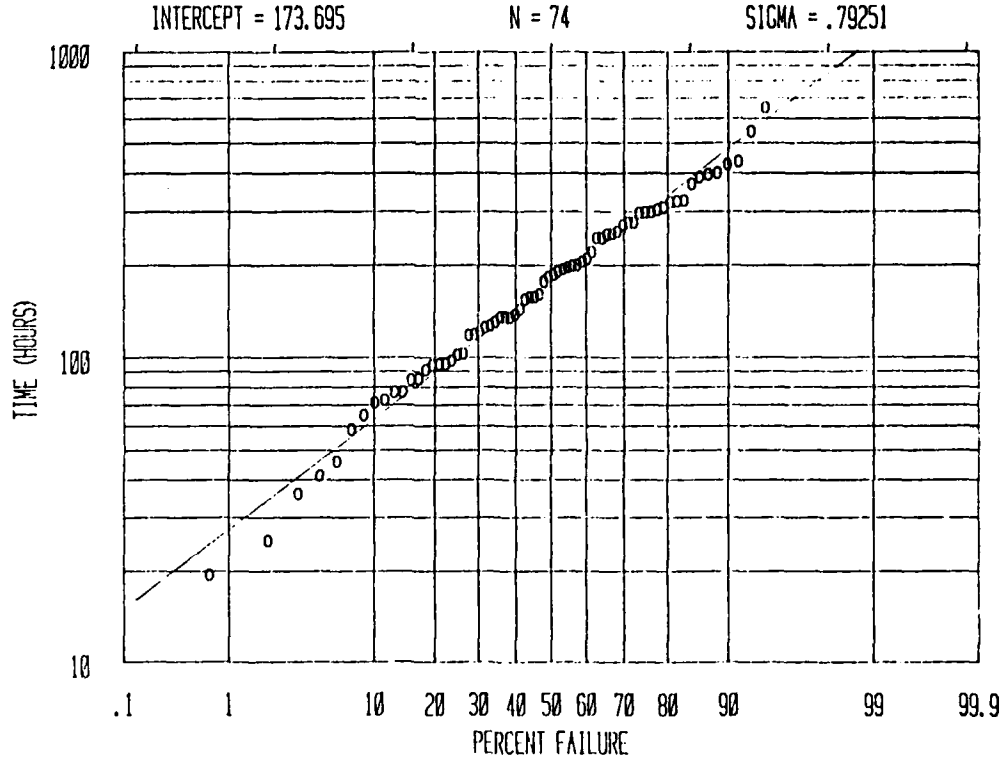


Figure 21. Test 1 Time (Hours) vs. Percent Failure for String 1

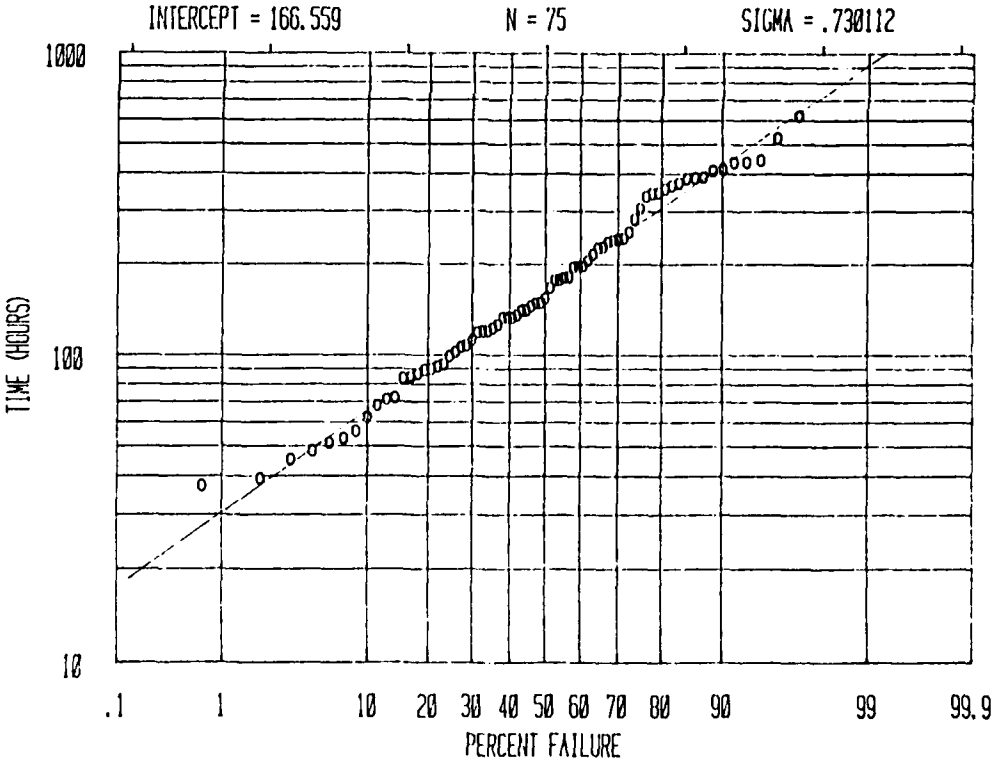


Figure 22. Test 1 Time (Hours) vs. Percent Failure for String 2

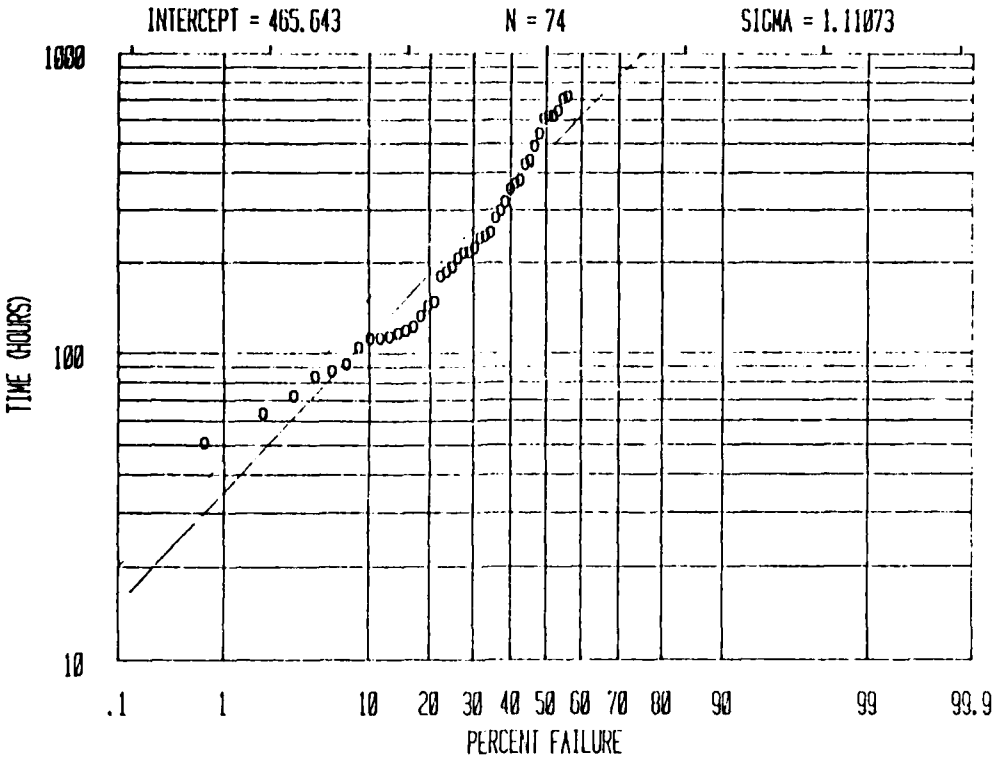


Figure 23. Test 1 Time (Hours) vs. Percent Failure for String 3

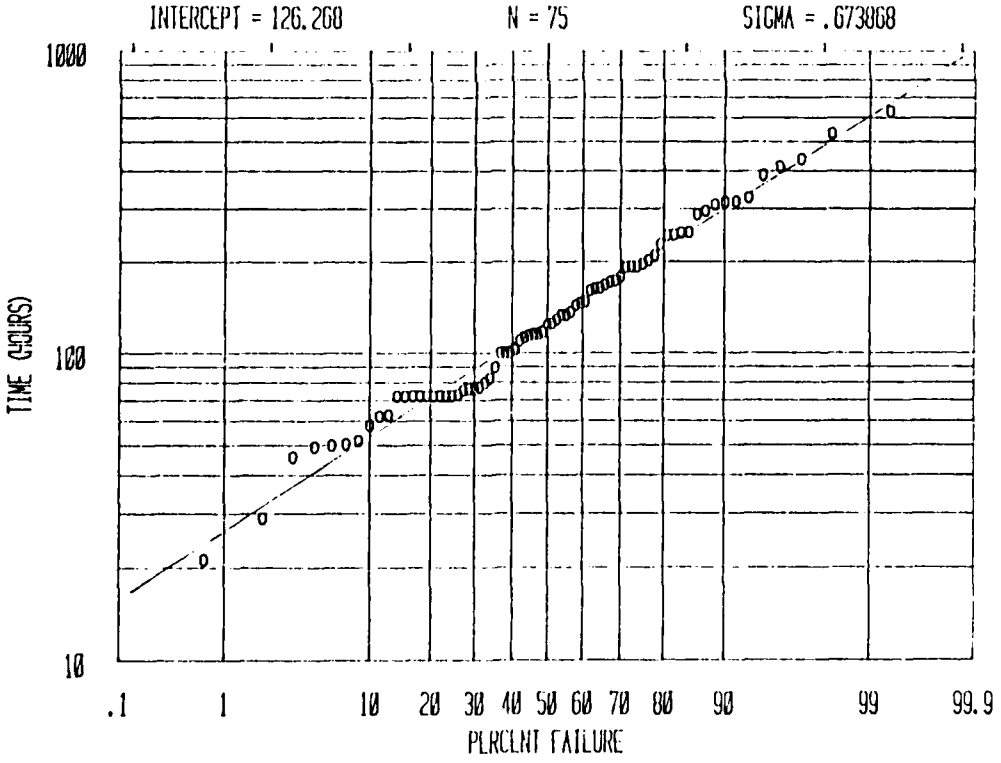


Figure 24. Test 1 Time (Hours) vs. Percent Failure for String 4

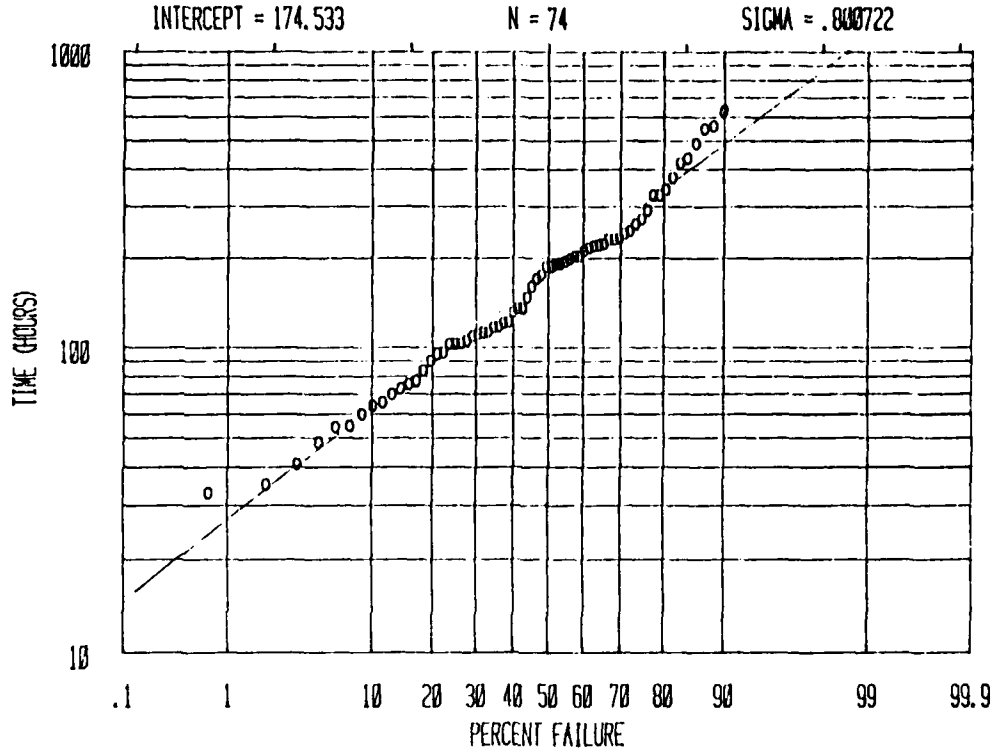


Figure 25. Test 2 Time (Hours) vs. Percent Failure for String 1

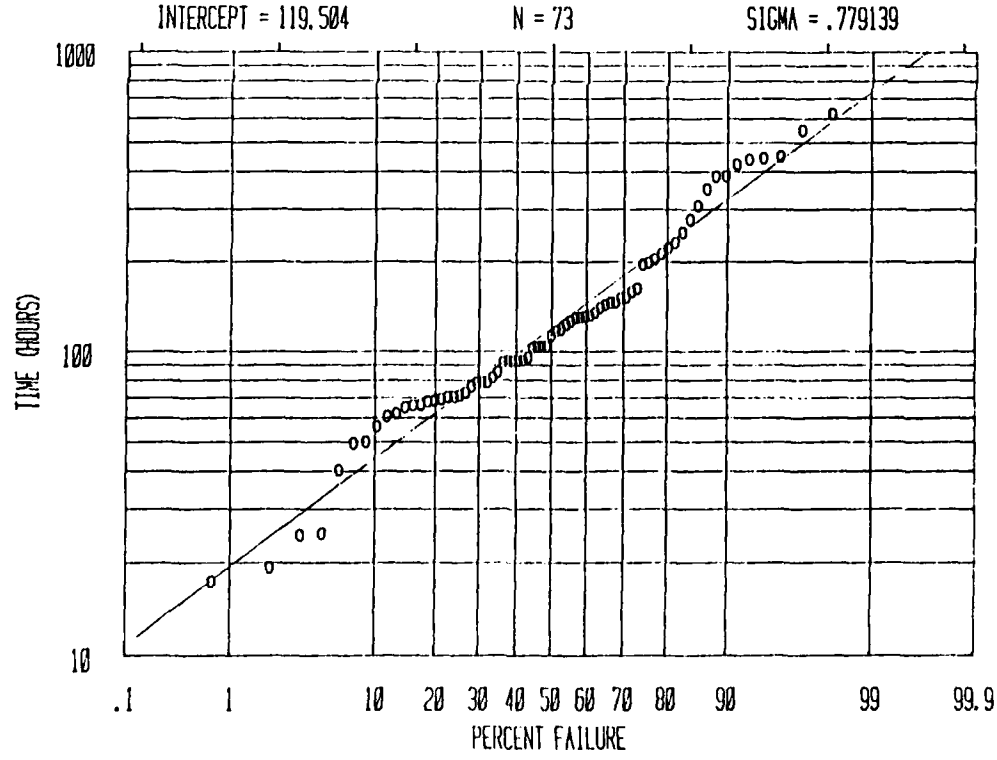


Figure 26. Test 2 Time (Hours) vs. Percent Failure for String 2

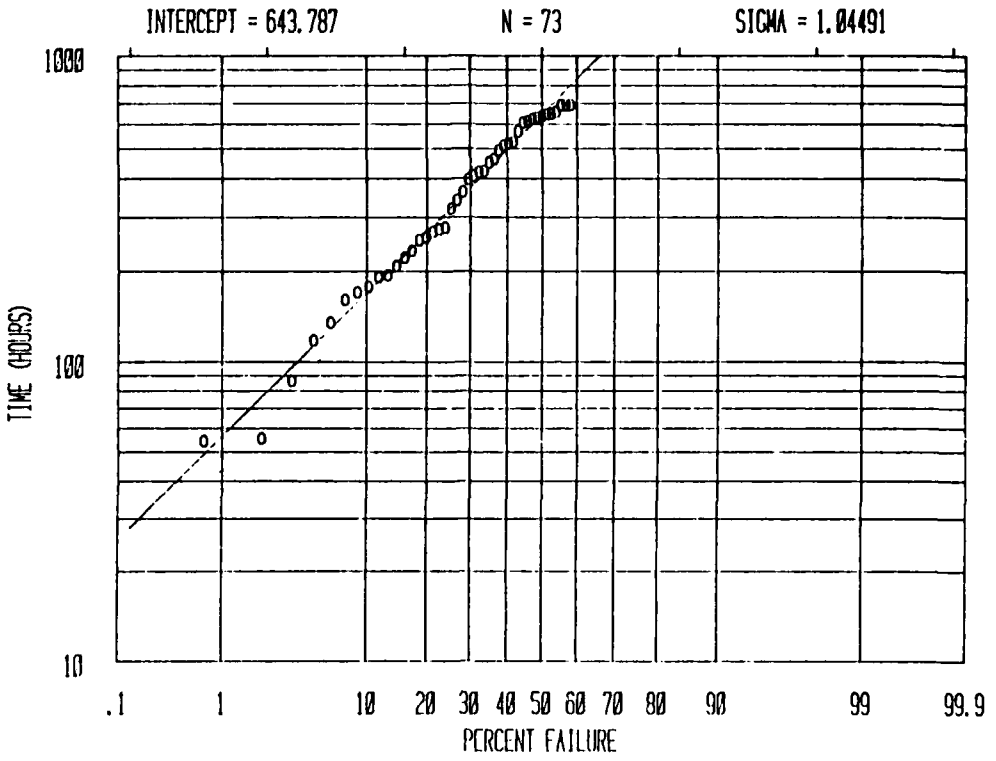


Figure 27. Test 2 Time (Hours) vs. Percent Failure for String 3

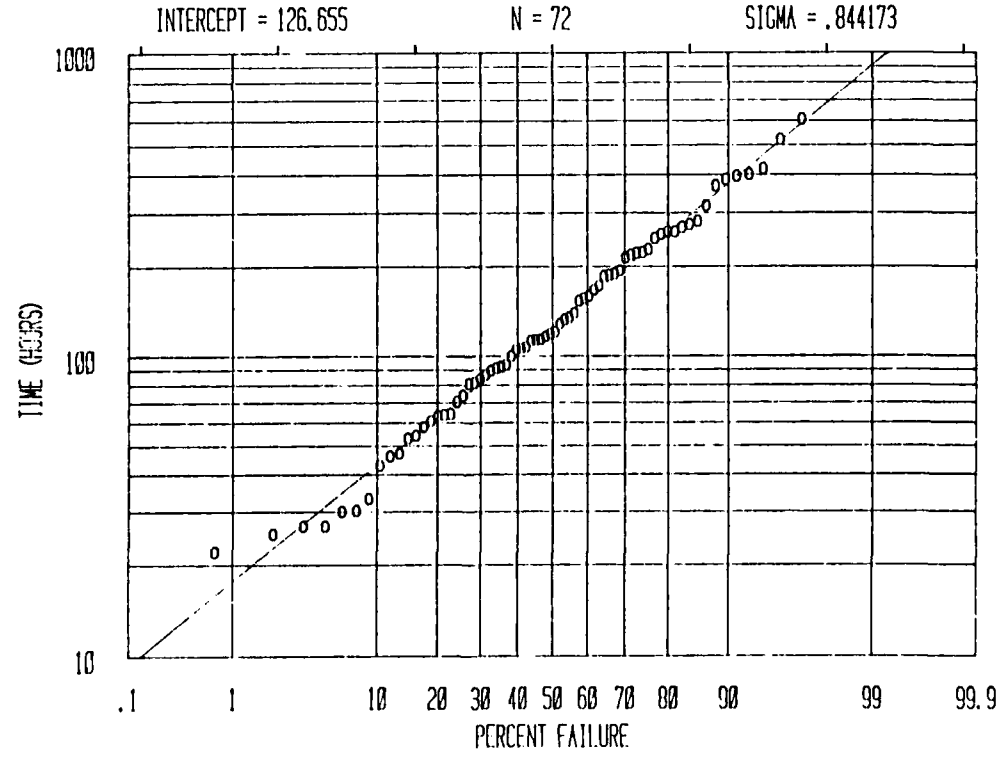


Figure 28. Test 2 Time (Hours) vs. Percent Failure for String 4

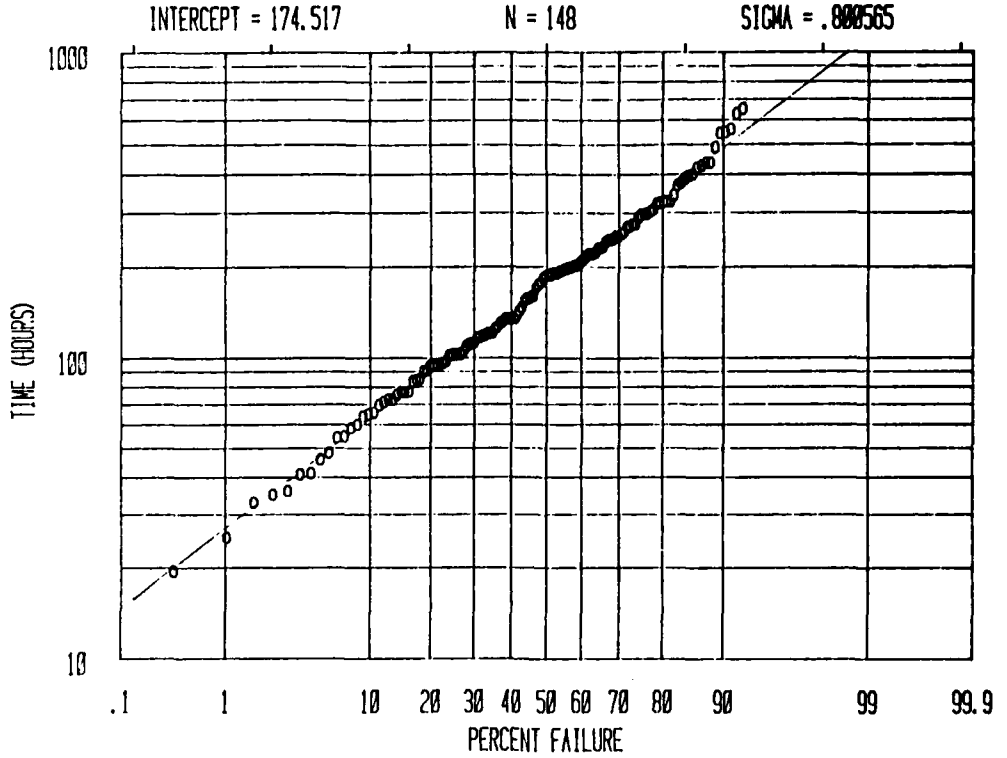


Figure 29. Test 1 and Test 2 Combined Time (Hours) vs. Percent Failure for String 1

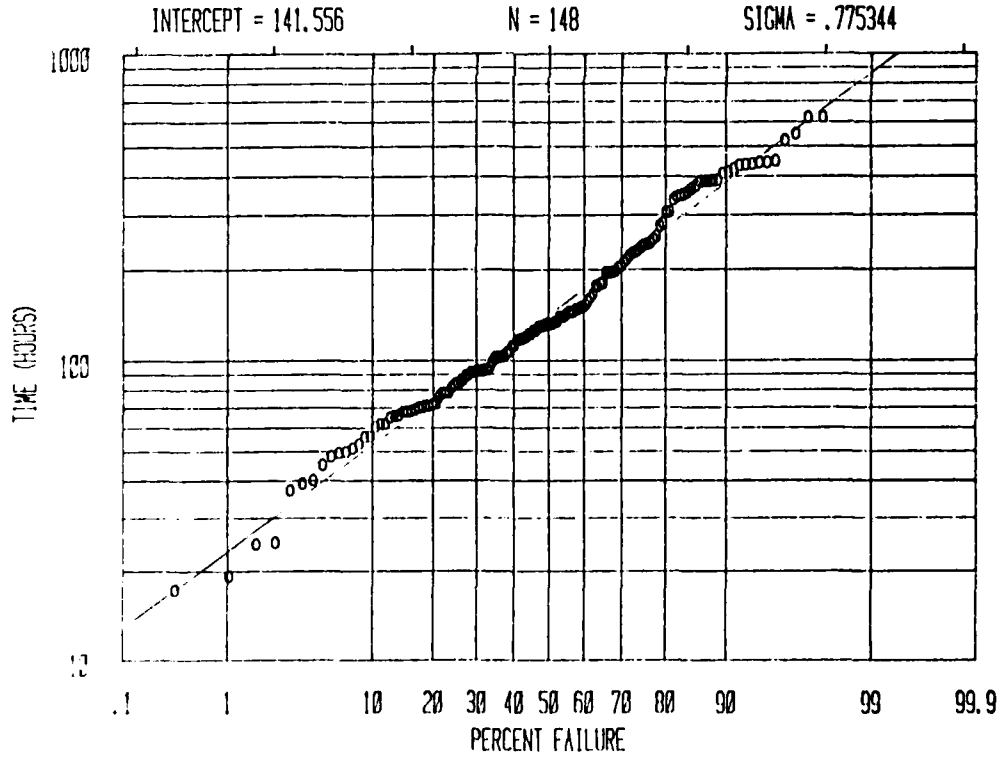


Figure 30. Test 1 and Test 2 Combined Time (Hours) vs. Percent Failure for String 2

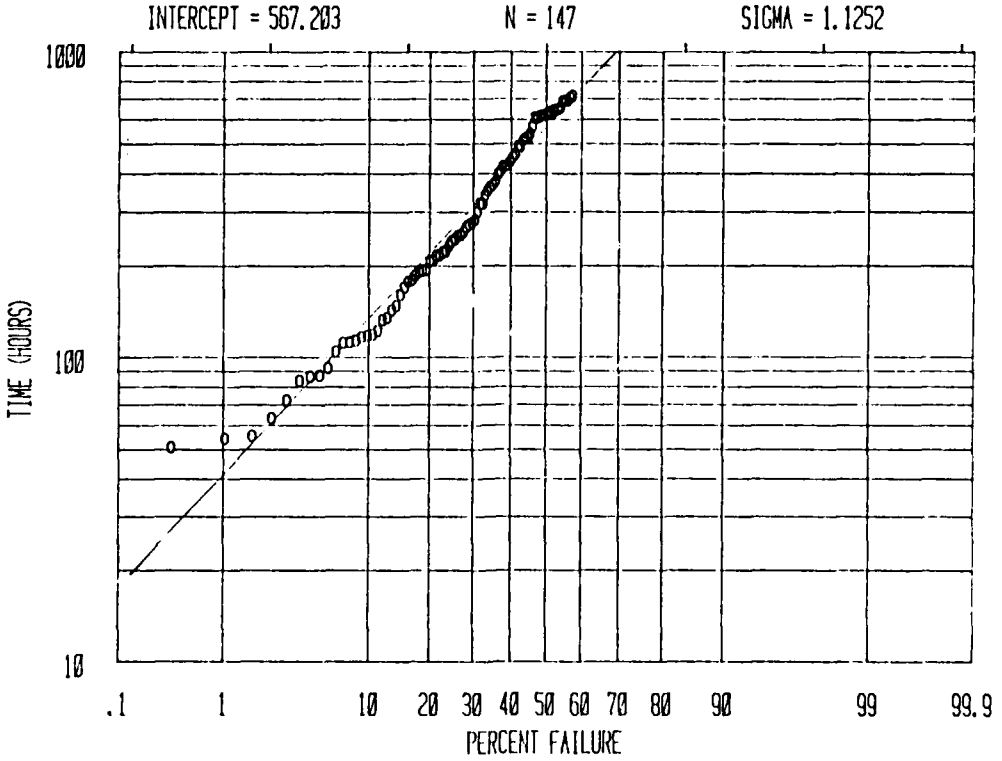


Figure 31. Test 1 and Test 2 Combined Time (Hours) vs. Percent Failure for String 3

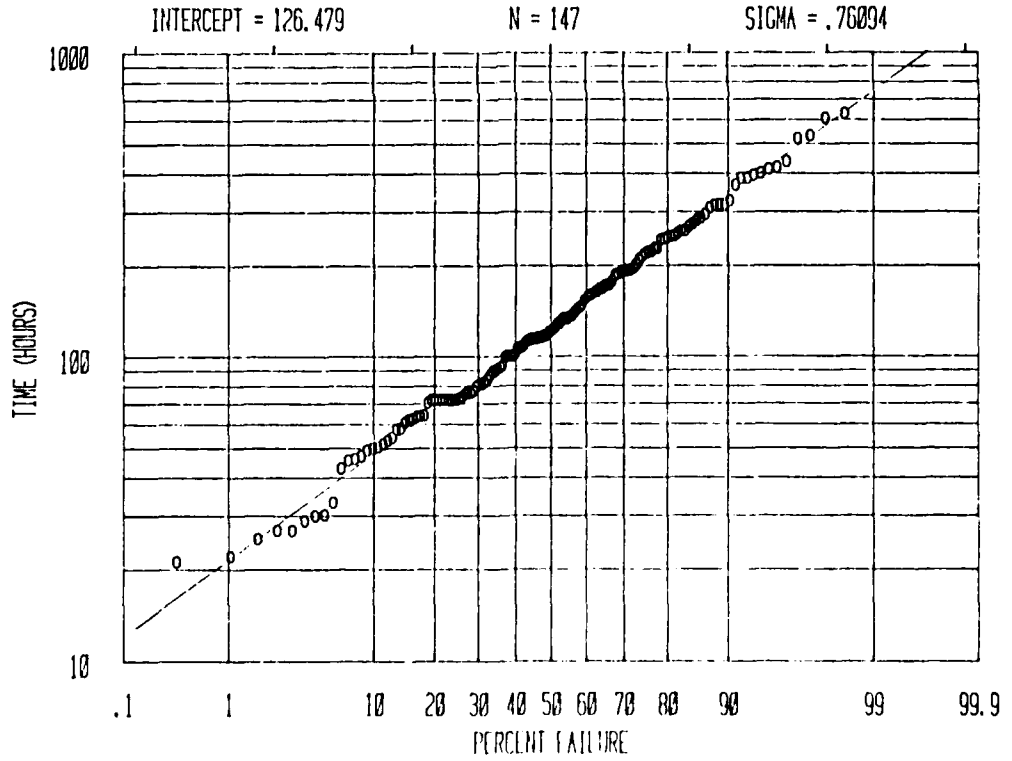


Figure 32. Test 1 and Test 2 Combined Time (Hours) vs. Percent Failure for String 4

4.7.1 Cumulative Distribution of Time-to-Failure

All of the distribution for the two tests except the first tests of the type 3 line fit a log normal distribution quite well over the whole range failure percentages. For the combined data the fit is even better, including the data for the type 3 line. These results indicate that the log normal distribution is valid at least down to the 0.3% point. The sample size and σ are large enough that any differences between log normal, logarithmic extreme value, and normal distribution would be evident.

4.7.2 Line Length Dependence

Since lines 1 and 4 both have the same width and lengths of 200 μm and 1650 μm respectively, Figures 29 and 32 may be used to assess the impact of line length on the distribution of times to failure. Both the t_{50} and σ are significantly reduced by increasing line length, as expected.

A simplified statistical model may be used to explain these results. Consider that the test line is made up of N identical sub-elements of length ΔL connected in series and failure of a line occurs whenever any one element fails. Let $r_{\Delta L}(t)$ be the reliability of an individual sub-element at time t, i.e., the probability that the sub-element will survive to time t. If we assume that all of the elements are statistically independent of each other, the reliability for the line is given by,

$$R(t) = (r_{\Delta L}(t))^{N}$$

$$= (r_{\Delta L}(t))^{L/\Delta L} \qquad (8)$$

where N = the number of elements in the line = $L/\Delta L$, where L is the line length. Expressing the reliabilities as the complement of the cumulative failure distributions, we have,

$$F(t) = 1 - (1-\rho_{\Delta L}(t))^{L/\Delta L} . \qquad (9)$$

where F(t) and $\rho_{\Delta L}(t)$ are the cumulative failure probabilities for the line and the elements, respectively. If we have two lines of lengths L_1 and L_2, their cumulative distributions are related by,

$$F_2(t) = 1 - (1-F_1)^{\frac{L_2}{L_1}} . \qquad (10)$$

Using Equation (10) the cumulative distribution for any length of line may be estimated if the distribution for any other length line is known. In Figure 33 the cumulative distributions are plotted for several different line lengths, assuming Equation (10) is valid and that the distribution for the 1650 μm line is that of Figure 32. The data for both the 1650 μm line and the 200 μm line are also plotted for comparison.

It is evident that for the assumed statistical model, if a distribution is log-normal for one line length it will not be log normal for another. In fact, one would expect that the failure distribution is log-extreme value for any length. However, our data fits a log normal distribution for all lengths, which indicates that the assumed statistical model is invalid. Since the model is based on the assumption that the failure times of the sub-elements are statistically independent, we can conclude that the probabilities of failure of different sub-elements in the same line are correlated. This is a reasonable inference since line-to-line variations in width, thickness, and temperature will tend to cause positive correlation between times-to-failure of the sub-elements of a given line.

Figure 33 shows that the data is in substantial agreement with the simplified model for low failure percentages. Therefore, Equation (10) may be used to determine the approximate variation of t_{50} and σ with line length. The variation of t_{50} with line length is shown in Figure 34 and that of σ is shown in Figure 35. Both the t_{50} and σ may be expected to decrease substantially as the length increases. The t_{50} decreases as $\sqrt{L}$ for $L > 1000$ μm. The σ decreases from 1.2 for a 200 μm line to 0.5 for a 15,000 μm line. Therefore, the use of long lines, greater than 10,000 μm, is advantageous for life testing since both the life test duration may be decreased and the number of samples required to project to early failure may also be decreased.

4.7.3 Correlation Between Failure Time and Initial Resistance Change

As described in Section 4.4, the resistance of each line was measured frequently during its life and recorded in 1% intervals. Therefore, for each line a series of discrete resistance and time readings is available up to the point of failure. Figures 36 and 37 show examples of this data for the type 1 and 2 lines, respectively. While there is significant variation from sample to sample in the initial rate of rise of resistance, it does not appear to be well correlated with the failure time, as evidenced by the crossing of the different curves. Note that all of the samples fail very shortly after the resistance change reaches the 5-6% level.

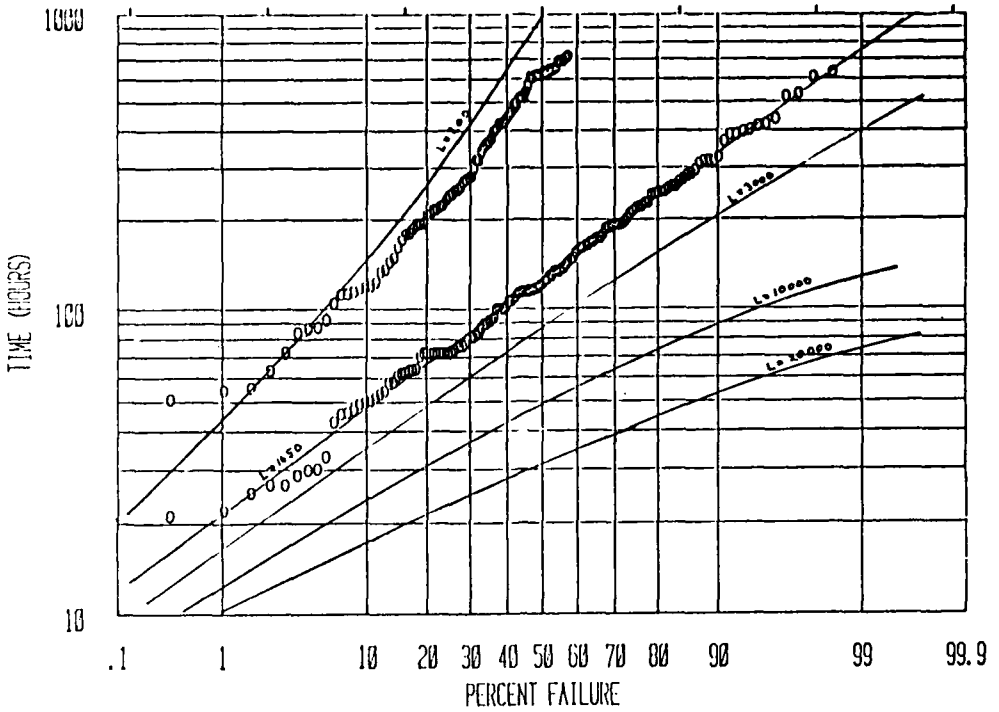


Figure 33. Comparing Calculated Distributions for Different Lengths with Data for Lines 3 and 4

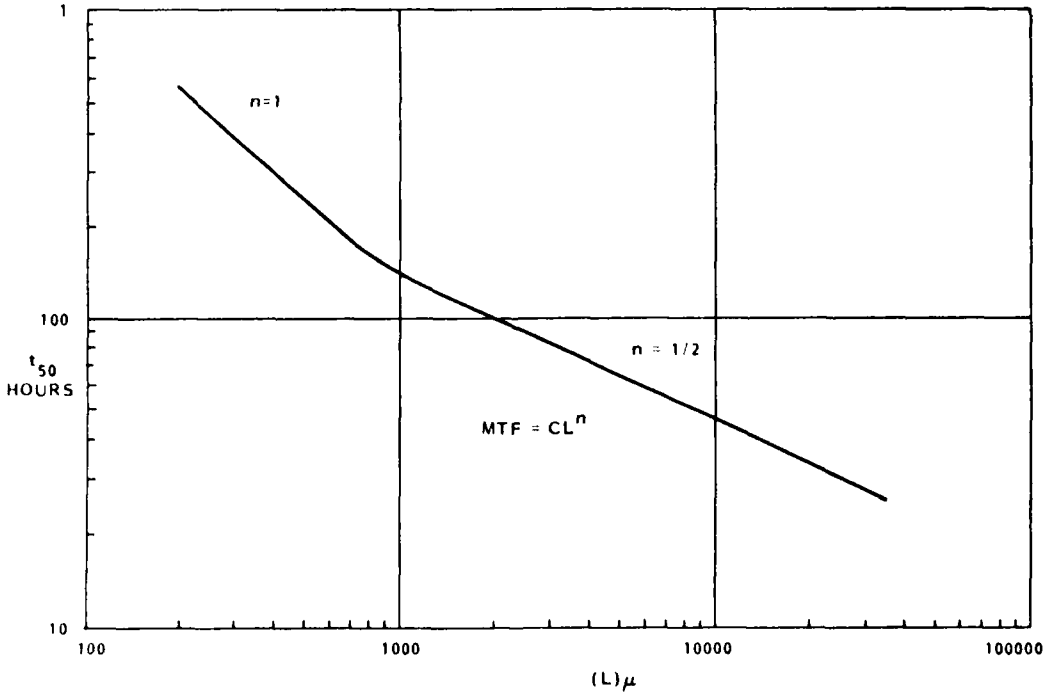


Figure 34. Dependence of t_{50} on Line Length

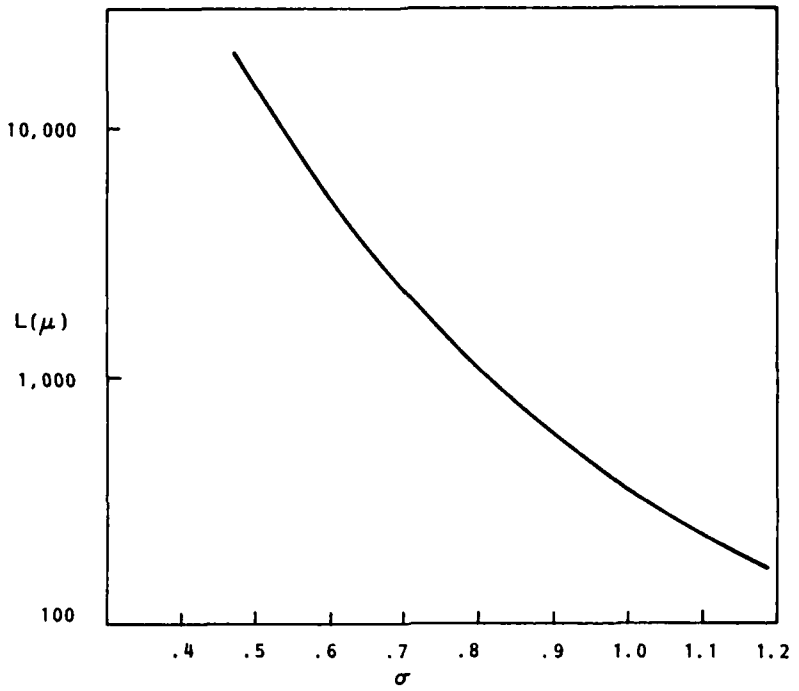


Figure 35. Dependence of σ on Linelength

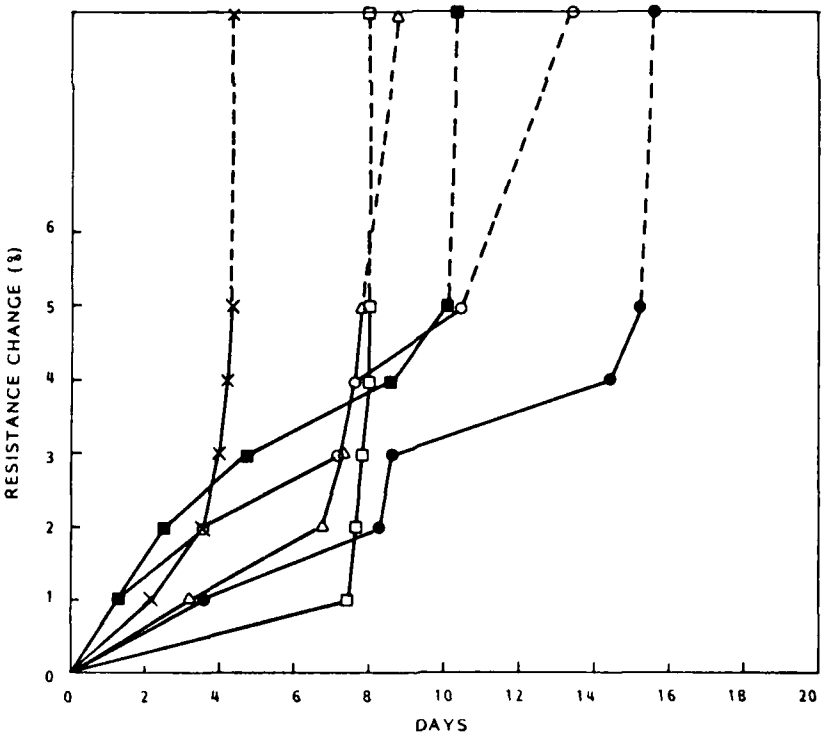


Figure 36. Line 1 - Resistance Change vs. Time

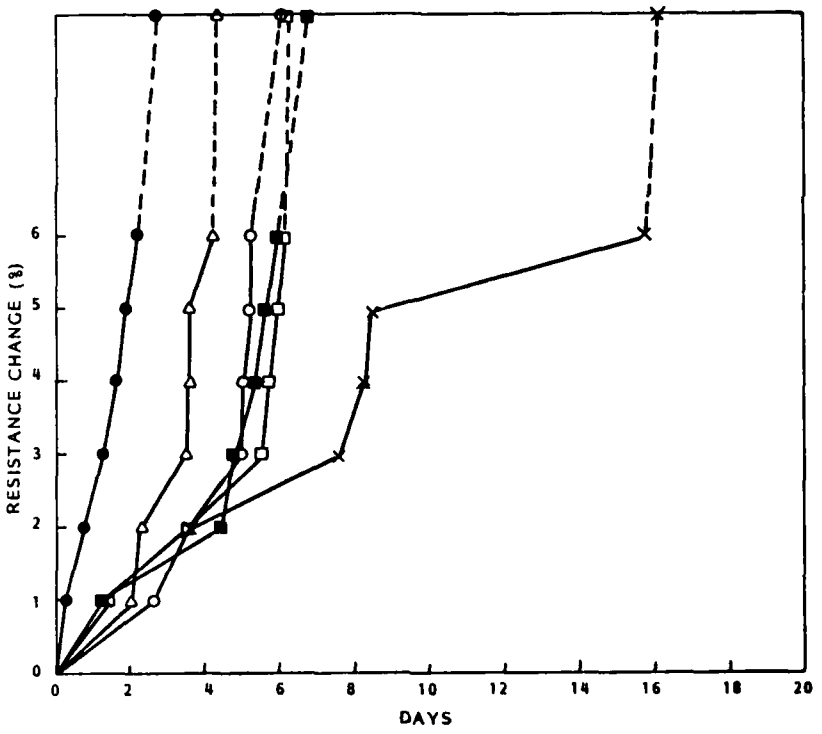


Figure 37. Line 2 - Resistance Change vs. Time

In order to evaluate this correlation more quantitatively, the correlation coefficient between the failure time and the time required for the resistance to change by X%, for various values of X was calculated. Data for twenty lines, selected at random, was used for this calculation. The results are presented in Figure 38 for the type 1, 2, and 4 lines. For all three lines the correlation between early resistance change and failure time is very low, approaching zero, and rises rapidly for higher percentage changes. At 5% change the degree of correlation is very high. This is evident from Figures 36 and 37 since failure occurs soon after the 5% point is reached. The results presented in Figure 38 are quantitative verification of the lack of correlation between early resistance changes and lifetime, reinforcing the conclusion of the exploratory tests that resistometric techniques are not valid for lifetime estimation.

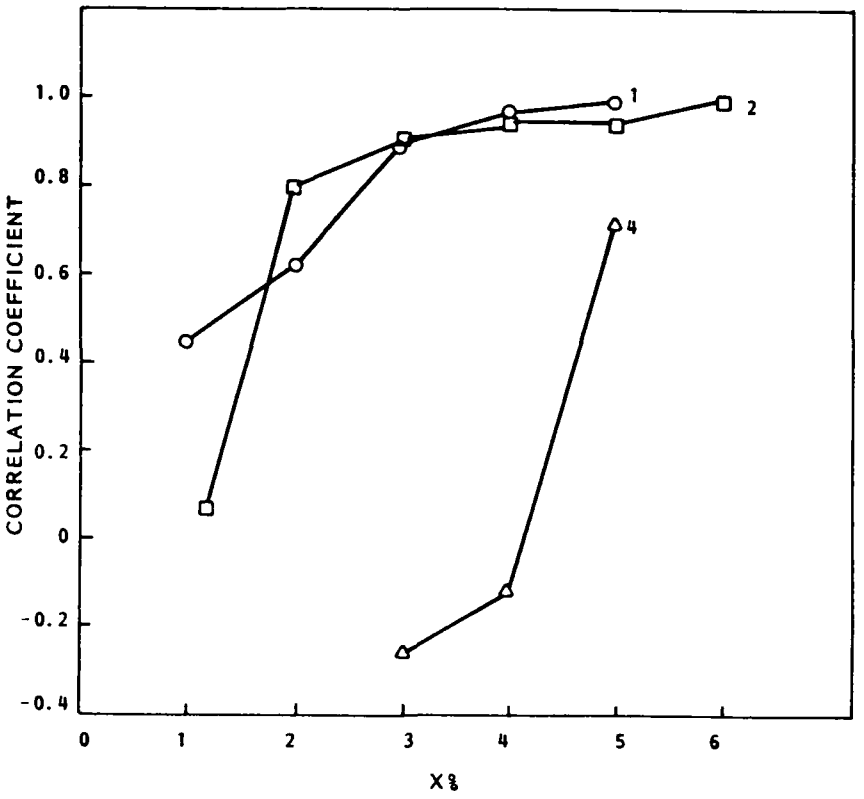


Figure 38. Correlation Between Failure Time and Time for Resistance to Increase by X%

5 AN APPROACH TO A STANDARD ELECTROMIGRATION TEST

5.1 INTRODUCTION

An electromigration test standard must have the following characteristics:

- It must be applicable to any candidate metallization system,
- It must be compatible with any microcircuit design and process technology,
- It must provide an accurate estimate for the time-to-first-failure,
- Realistic and acceptable criteria must be defined for acceptance or rejection,
- It must also be practical in terms of the time and effort required to implement it.

The development of such a test is not a trivial matter, primarily because of the flexiblity necessary to make it applicable under all circumstances to all metallizations and technologies. The experimental results obtained on the current program provide some valuable information necessary to define such a test method and other information is available in the published literature. More information needs to be developed to complete the task satisfactorily. Work is in progress at the National Bureau of Standards with the purpose of developing electromigration test standards and the results of that program will provide useful inputs to the desired qualification procedure. In addition, there is a large amount of work currently in progress in other laboratories exploring such vital issues as the current density dependence, and the behavior of submicron lines under high current density stress.

A prototype test procedure has been developed, based on the information available at this time. This procedure is presented as a first step in the process of the evolution of an acceptable test method. It provides a vehicle for discussion which may be modified as new information or insights become available. A summary of the procedure is contained in the Appendix. In this section of the report the test method is considered, section by section, and the rationale is given in some detail.

5.2 TEST SAMPLES

The test samples must be designed and processed to meet the following criteria:

1) *The test sample will consist of the meander pattern, shown in Figures A-1 and A-2.*

2) *If a two layer metallization system is being evaluated, a separate pattern will be prepared for each layer and will be tested separately.*

3) *The width of the line will be the minimum width allowed by the design rules for that level.*

4) *The total length of the narrow part of the line will be 32,000 μ meters.*

5) *The topology of the substrate must be such that the line crosses multiple worst case steps, as shown in Figure A-2.*

6) *Parallel extrusion monitors are provided on both sides of the line, separated from the line by the minimum line spacing allowed by the design rules.*

7) *The test patterns will be processed using the same procedures used for production wafers. It is preferred that the test chips be included as a test element on production wafers.*

8) *The metal thickness, insulator thicknesses, passivation thicknesses and thickness of the underlying oxide will be consistent with the technology being evaluated and the design rules and will be consistent with production practice.*

9) *The thermal annealing history of the samples will be identical to that seen in production processing.*

10) *The samples to be tested must be from at least three metallization lots, in equal quantity from each lot.*

11) *The samples will be mounted in hermetic packages very similar or identical to the production circuits using the same die mount as production circuits and same thermal exposure as sustained during production packaging. The package ambient will be consistent with production circuit.*

12) *There will be one test stripe per package.*

The above guidelines for designing a test sample were defined which specify only the length of the test stripe and general layout. The rest of the design is related to the design rules for the technology being evaluated, i.e. the minimum line width and separation, step size, etc. The length of 3.2 cm is justified on the basis of the results of this program which showed that the time to first failure of a very long line is the approximate equivalent

of the time to first failure of many shorter lines in series. Figure 39 is a histogram showing VLSI line length statistics, published by Ghate [10]. Essentially all of the interconnects have a length less than 500 μm. Therefore, a 3.2 cm test line is equivalent to 64 maximum length VLSI conductors. A sample quantity of 33 lines is, therefore, equivalent to approximately 2000 worst case VLSI conductors. This should a be a more than adequate sample size to determine the equivalent of the 0.1% failure time for the VLSI conductors.

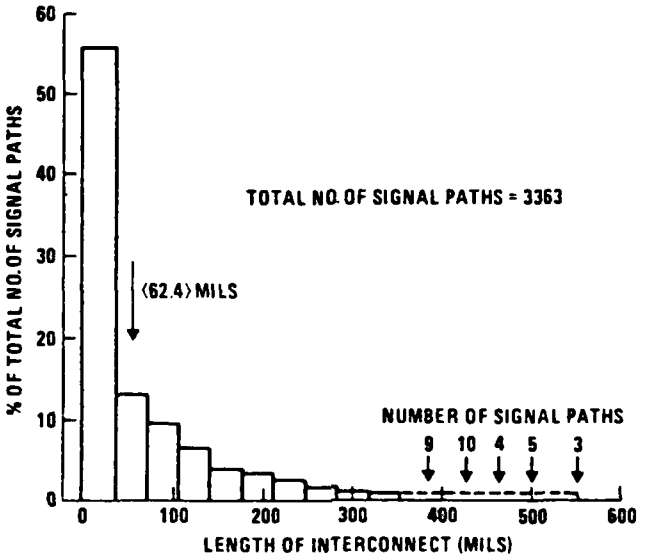


Figure 39. Histogram of Signal Path Lengths for a VLSI Circuit (From Reference 13)

The requirement that the test stripes cross multiple worst case steps is justified since the current density at the steps is higher due to the thinning of the metal over the steps. Parallel extrusion monitors are needed to detect lateral shorts which can be a major cause of failures in structures with thick glass or nitride coatings.

The requirement that samples originate from at least three metallization lots is meant to account for the large lot-to-lot variations observed in the time-to-failure due to electromigration.

Only one stripe per package is allowed since the thermal interaction between two samples in the same package can result in dependence between the failure times of the two samples, which is to be avoided.

5.3 LIFE TEST CIRCUIT

The test samples shall be stressed using the circuit shown in Figure 3. Multiple test samples may be connected in parallel to the same voltage source. The current limiting resistor, R_B, must be at least 11 times the test stripe resistance at the test temperature. The values of R_B for the different lines will be the same to within 1%. The resistor, R_B, will be located outside of the test chamber in a sufficiently stable thermal environment and will have a sufficiently large power rating that its value will not change more than 1% as the current is varied over its expected range. The supply voltage, V_S, will be adjusted so that the average voltage drop, V_L, across the Kelvin contacts, is,

$$V_L = \rho \; j\ell \qquad (A\text{-}1)$$

where ρ = *the average metal resistivity,*

j = *the current density at which the test is to be run,*

ℓ = *the line length = 3.2 cm.*

The specified test circuit of Figure A-3 is a convenient and simple means of monitoring both the test stripe and the extrusion monitor. If R_B is 11 times the line resistance, then a doubling of the stripe resistance (the failure criteria) results in a 10% reduction in current, an acceptable change over the duration of the life test. Because of the length of the lines and the relatively high voltage drop across the lines, schemes in which multiple lines are stressed in series are not practical.

The technique of first measuring the metal resistivity, ρ, and then using Equation (A-1) to control the average current density makes it possible to automatically compensate for line-to-line variations in metal cross section. This scheme will work as long as the resistivity does not vary significantly from line to line.

5.4 TEMPERATURE

The test samples will be mounted in a temperature chamber capable of maintaining the ambient temperature within ± 1°C across the array of unpowered test samples. Thermocouples mounted between the test sample package and its socket will be used to continuously monitor ambient temperature. At least 3 thermocouples will be used, one in the center of the array of samples, and 2 at opposite sides of the array. If a 3 dimensional array is used, one thermocouple must be located at the top of the array and one at the bottom. The ambient temperature is defined as the average of the thermocouple readings.

The self-heating by the test samples will be measured as follows:

- *With the samples mounted in the test chamber, the ambient temperature is brought up to within 25°C of the desired life test temperature.*
- *A low level current ($j < 1 \times 10^5$ A (cm^2)) is applied to the samples and the resulting values of V_L and V_R are measured for each sample.*
- *The resistance of each test line is calculated as*

$$R_L = \frac{V_L \times R_B}{V_R} \qquad (A\text{-}2)$$

and the average calculated.

- *The current is raised to that at which the life test is to be run and the temperature allowed to stabilize.*
- *The values of V_L and V_R are measured for each sample and R_L is calculated and averaged.*
- *If the resulting average resistance is higher than the initial value, the test chamber is allowed to gradually cool and stabilize at a lower temperature level and a new average resistance measured. The procedure is continued until the average resistance is within 1°C of the original low current level.*
- *The self-heating is defined as the decrease in the ambient temperature required to make the average resistance at the high current condition coincide with that measured at the low current condition.*

The maximum sample temperature will be 200°C. The sample temperature is defined as the sum of the ambient temperature and the measured self-heating. Lower temperatures may be chosen for the life test, but this will extend the required test duration, as described in Section 5.2.

The technique specified for measuring the self-heating is very convenient when the average self-heating for multiple lines is to be measured. The assumption is made that the resistivity depends only on temperature and not on current, but a linear temperature dependence is not assumed.

The definition of ambient temperature as the average of the temperature readings of several thermocouples placed throughout the array of test samples is arbitrary. It might also be defined as the temperature of the incoming circulating air, or other convenient reference.

5.5 SAMPLE QUANTITY

At least 33 test samples will be subjected to life test.

The minimum sample size must be large enough to insure that the estimate of the time for 5% of the lines to fail is reasonably accurate. The justification for estimating the 5% failure point, instead of the 0.1% point is given below in Section 5.10. If we assume that we have 33 samples with a log-normal distribution and with a $\sigma = 1$, we will have 90% confidence that our estimated $t_{5\%}$ is no more than 37% higher than the actual value. For $\sigma = 0.5$ the anticipated error is 17%, again with 90% confidence. Our life test results indicated that very long lines will have a $\sigma < 0.5$. However, these results were based on tests of samples from the same wafer and lot. Lot-to-lot and wafer-to-wafer variations may be expected to increase σ somewhat. The recommended quantity of 33 is adequate to insure that the estimated $t_{5\%}$ is well within a factor of two of the actual value, even for values of σ in excess of 1.0.

5.6 DUTY CYCLE

The duty cycle should be at least as high as the maximum duty cycle experience in use. A CW life test will result in minimum required test duration, as described in Section 5.2.

Time-to-failure decreases as the duty cycle decreases and many VLSI microcircuits operate at a relatively small duty cycle. Therefore, provision is made in the test procedure to take into consideration the deceleration of the electromigration process. Most observers have reported that the decrease with duty cycle is superlinear. A linear dependence is assumed here (Equation A-6), a conservative assumption.

5.7 FAILURE DEFINITION

A sample will be defined as having failed if V_L increases by 100% or more, or if V_m exceeds 10 mV.

The definition of a failure as a 100% increase in line resistance is arbitrary but reasonable. For many test stripes open circuit failure occurs well before the 100% change is observed. The two test samples tested on this program failed after 20% and 6%, respectively. Rodbell and Shatynski [11] have proposed the 100% failure criteria.

The choice of 10 mV as the maximum voltage allowed on the monitor stripe implies that the maximum leakage current across an extrusion will be 10 nA, a reasonable limiting value.

5.8 CURRENT DENSITY

The current density must be at least as high as the maximum current density for which the metallization system is to be qualified. If a higher current density is used, the test duration may be reduced, as described in Section 5.2.

It is required that the test be run at a current density which is at least as high as that for which the metallization system is to be qualified because of the uncertainty in extrapolating from lower to higher current densities. If the test is run at higher than the design value, a current density dependence of $j^{1.5}$ is assumed, a conservative value consistent with the recommendations of Ghate [10] and the recent measurements of Schafft et al [12].

5.9 DURATION OF TEST

The life test will be continued until at least fifty percent of the samples have failed or until t_m hours, whichever is smaller. The time, t_m, is given by

$$t_m = k \times t_{crit.} \qquad (A\text{-}4)$$

where $t_{crit.}$ is the required time to first failure defined in Section 5.2 and where k is plotted in Figure A-2 as a function of σ. The value of σ used to determine k is estimated using the failure times for the samples which have failed.

At least fifty percent of the samples are required to fail during the test in order to insure that enough data points are obtained to define the distribution and extrapolate to the 5% point with confidence. If the metallization system is so resistant to electromigration that one-half will not fail in a reasonable time, the test should be truncated. The time after which it is safe to assume that the metallization system is qualified was estimated as follows:

The ratio, r, of the $t_{50\%}$ to the $t_{5\%}$ for a log-normal distribution is plotted in Figure 40 as a function of σ. If σ is known and if one-half the samples have not failed by a time t_m, then we know that $t_{5\%} > t_m/r$. Therefore, we can be sure that $t_{5\%} > t_{crit.}$ if

$$t_{crit.} = \frac{t_m}{r} \qquad (5\text{-}4)$$

or

$$t_m = r \times t_{crit.} \qquad (5\text{-}5)$$

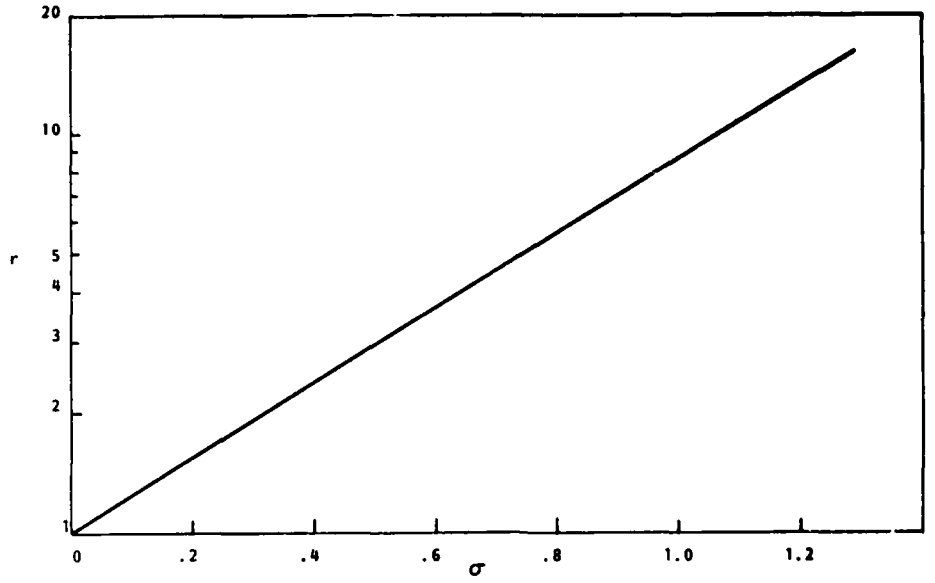


Figure 40. Ratio of $t_{50\%}$ to $t_{5\%}$ for Log-Normal Distribution

Since σ is not known but is estimated from the data that is available, we have defined k = 2r to provide margin for error. The values of r and k obtained from Figures 40 and (A-4), respectively, vary by this factor of two.

5.10 ACCEPTANCE CRITERIA

The metallization system will be considered qualified for use at current density, j_o, if the estimated value of $t_{5\%}$, obtained as described above, is larger than $t_{crit.}$ where $t_{crit.}$ is defined by

$$t_{crit.} = 1000 \left(\frac{j}{j_o}\right)^{1.5} \cdot \frac{d_o}{d} \cdot \exp\left[\frac{0.5}{k}\left(\frac{1}{T} - \frac{1}{398}\right)\right] \text{ hrs.} \qquad (A\text{-}6)$$

where j = *the test current density*

j_o = *the maximum current density for which the metallization system is qualified* ($j_o \leq j$)

d_o = *the maximum duty cycle in use*

d = *the life test duty cycle*

T = *the metallization temperature during the life test defined in 4.3.2*

and k = *Boltzmann's constant.*

Since the maximum duration of the life test depends on $t_{crit.}$, (Equation 4), the required duration may be controlled by the proper selection of j, d, and T.

If 50% of the samples have not failed by t_m, and if the first failure (n = 1) occurred after $t_{crit.}$, the metallization system is considered qualified for use at j_o.

Our criterion for qualification of the metallization system is based on the current MIL-STD-883C microcircuit qualification requirement, i.e. the first failures must occur after the equivalent of 1000 hours at 125°C. Equation (A-6) is consistent with this requirement.

We have defined the time to first failure as the 0.1% failure time. However, since the test samples are much longer than the conductors to be found in VLSI circuits, it may be expected that their failure times will be shorter than those of VLSI conductors.

We have seen that the following relationship between the cumulative failure distribution of two lines of different lengths is approximately valid,

$$F_1(t) = 1-(1-F_2(t))^{L_1/L_2} \qquad (5\text{-}6)$$

For $F_2(t) << 1$, Equation (5-6) is approximated by,

$$F_1(t) = \frac{L_1}{L_2} F_2(t) \qquad (5\text{-}7)$$

Based on reference [10], the maximum length of conductors in a VLSI microcircuit is approximately 500 μm. If we assume that $F_2(t)$ is the cumulative percent failures for these 500 μm long lines and that is equal to 0.1%, Equation (5-7) may be used to estimate the equivalent cumulative failure percentage for the test stripes, which are 32,000 μm long:

$$F_1(t) = \frac{32,000}{500} \times 0.1\% = 6.4\% \qquad (5\text{-}8)$$

Therefore, the failure of 6.4% of our test samples is equivalent to 0.1% failures of worst case VLSI conductors. For convenience, in the test method we have based the acceptance criteria on the time required for 5% of the test samples to fail.

6 SUMMARY AND CONCLUSIONS

Several approaches for implementing a standard test for qualifying VLSI metallization systems have been evaluated. The use of resistometric methods to predict stripe life based on early resistance changes has been found to be inadequate because of lack of correlation between these changes and time-to-failure. It has been found that the failure of a metal stripe is the result of a sequence of events, including void formation and growth, void dynamics, possible arcing across voids, and interaction between temperature fluctuations and voids. The life time of a line can be more a function of the ability of a line to heal than of the initial rate of change of resistance.

The times-to-failure of the metal stripes tested on this program were log-normally distributed down to the 0.2% failure point, for all of the line lengths tested.

The dependence of the distribution of times-to-failure on line length was found to be approximately that predicted by a model in which a long line is considered statistically equivalent to many short lines in series. The data deviates from the model predictions for failure percentages in excess of 10%, indicating that some correlation exists between the probabilities of failure of different segments of the same line. However, the agreement between the data and model is good enough for early failures that a long line may be considered as statistically equivalent to many short lines when measuring time-to-first-failure. Therefore, a life test in which a modest number of very long lines are tested can be used to measure the time for very early failures ($< 0.1\%$).

A first-cut electromigration test method has been developed, based on this approach.

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APPENDIX

A TEST METHOD FOR VLSI METALLIZATION QUALIFICATION

ELECTROMIGRATION RESISTANCE

1.0 PURPOSE

The purpose of this test method is to determine the susceptibility of a microcircuit metallization system to electromigration and to define the maximum acceptable design current density which may be used with that metallization system.

2.0 APPROACH

A standard life test is to be run using test samples which are prepared using the production processing and materials. The test circuit is designed following the specific guidelines described below. The quantity of circuits tested, the test procedures, and the acceptance criteria are all defined by the test method. The current density stress may be varied, depending on the maximum current density for which the metallization system is to be qualified. If the results of the test demonstrate that the system meets the acceptance criteria, the metallization system is considered qualified for that maximum current density and microcircuit design rules allowing that maximum current density may be used. If the acceptance criteria are not met, the test may be repeated for a lower current density. Documentation must be maintained to demonstrate that the sample design, test procedures, and results are consistent with this test method.

3.0 TEST SAMPLES

The test samples must be designed and processed to meet the following criteria:

1) The test sample will consist of the meander pattern, shown in Figures A-1 and A-2.

2) If a two layer metallization system is being evaluated, a separate pattern will be prepared for each layer and will be tested separately.

3) The width of the line will be the minimum width allowed by the design rules for that level.

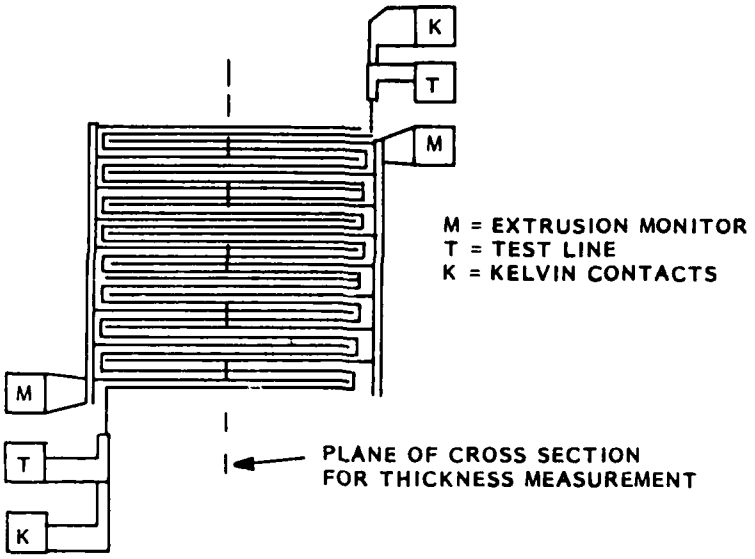

Figure A-1. Electromigration Test Sample

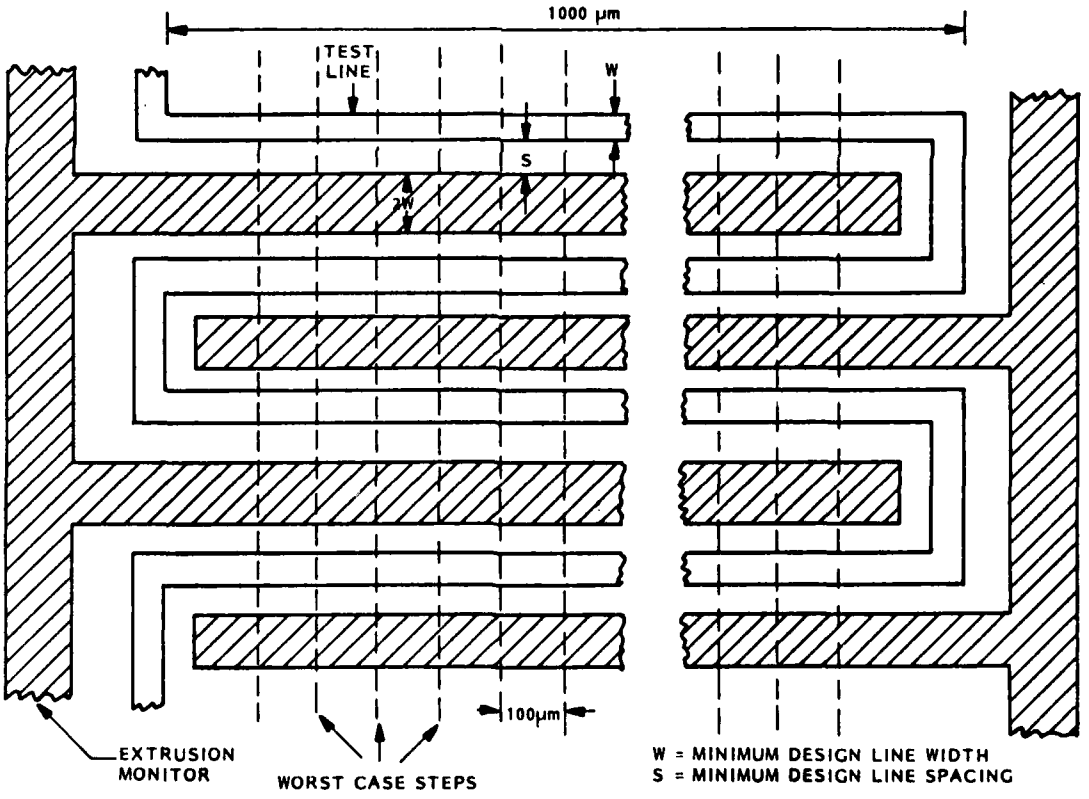

Figure A-2. Layout Details of Electromigration Test Sample

4) The total length of the narrow part of the line will be 32,000 μ meters.

5) The topology of the substrate must be such that the line crosses multiple worst case steps, as shown in Figure A-2.

6) Parallel extrusion monitors are provided on both sides of the line, separated from the line by the minimum line spacing allowed by the design rules.

7) The test patterns will be processed using the same procedures used for production wafers. It is preferred that the test chips be included as a test element on production wafers.

8) The metal thickness, insulator thicknesses, passivation thicknesses and thickness of the underlying oxide will be consistent with the technology being evaluated and the design rules and will be consistent with production practice.

9) The thermal annealing history of the samples will be identical to that seen in production processing.

10) The samples to be tested must be from at least three metallization lots, in equal quantity from each lot.

11) The samples will be mounted in hermetic packages very similar or identical to the production circuits using the same die mount as production circuits and some thermal exposure as sustained during production packaging. The package ambient will be consistent with production circuit.

12) There will be one test stripe per package.

4.0 TEST PROCEDURES

4.1 Resistivity Measurements

The sheet resistance of the metallization at room temperature (25°C) will be measured for each chip using a suitable 4-terminal test structure to be included on each chip with the test pattern. Samples from each wafer from which tests samples are taken will be cross-sectioned perpendicular to the long dimension of the meander, as shown in Figure 1. The thickness of the metal layer will be estimated using SEM measurements and an average thickness for the test samples will be obtained by averaging the estimates for each wafer. The metal resistivities will be calculated as the product of the average sheet resistance and the average thickness.

4.2 Life Test Circuit

The test samples shall be stressed using the circuit shown in Figure A-3. Multiple test samples may be connected in parallel to the same voltage source. The current limiting resistor, R_B, must be at least 11 times the test stripe resistance at the test temperature. The values of R_B for the different lines will be the same to within 1%. The resistor, R_B, will be located outside of the test chamber in a sufficiently stable thermal environment and will have a sufficiently large power rating that its value will not change more than 1% as the current is varied over its expected range. The supply voltage, V_S, will be adjusted so that the average voltage drop, V_L, across the Kelvin contacts, is,

$$V_L = \rho \; j \ell \qquad \text{(A-1)}$$

where ρ = the average metal resistivity,

j = the current density at which the test is to be run,

ℓ = the line length = 3.2 cm.

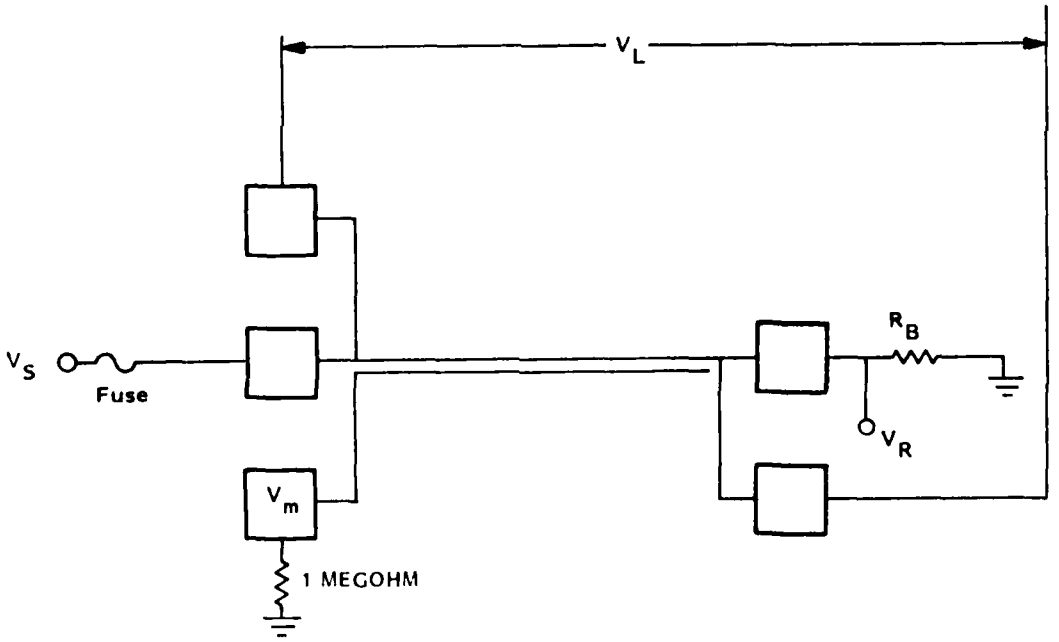

Figure A-3. Life Test Arrangement for Single Stripe

4.3 Temperature Control

The test samples will be mounted in a temperature chamber capable of maintaining the ambient temperature within ± 1°C across the array of unpowered test samples. Thermocouples mounted between the test sample package and its socket will be used to continuously monitor ambient temperature. At least 3 thermocouples will be used, one in the center of the array of samples, and 2 at opposite sides of the array. If a 3 dimensional array is used, one thermocouple must be located at the top of the array and one at the bottom. The ambient temperature is defined as the average of the thermocouple readings.

The self-heating by the test samples will be measured as follows:

- With the samples mounted in the test chamber, the ambient temperature is brought up to within 25°C of the desired life test temperature.
- A low level current ($j < 1 \times 10^5$ A(cm^2)) is applied to the samples and the resulting values of V_L and V_R are measured for each sample.
- The resistance of each test line is calculated as

$$R_L = \frac{V_L \times R_B}{V_R} \qquad \text{(A-2)}$$

  and the average calculated.
- The current is raised to that at which the life test is to be run and the temperature allowed to stabilize.
- The values of V_L and V_R are measured for each sample and R_L is calculated and averaged.
- If the resulting average resistance is higher than the initial value, the test chamber is allowed to gradually cool and stabilize at a lower temperature level and a new average resistance measured. The procedure is continued until the average resistance is within 1°C of the original low current level.
- The self-heating is defined as the decrease in the ambient temperature required to make the average resistance at the high current condition coincide with that measured at the low current condition.

4.4 Life Test Parameters

4.4.1 Number of Samples

At least 33 test samples will be subjected to life test.

4.4.2 Temperature

The maximum sample temperature will be 200°C. The sample temperature is defined as the sum of the ambient temperature and the measured self-heating. Lower temperatures may be chosen for the life test, but this will extend the required test duration, as described in Section 5.2.

4.4.3 Duty Cycle

The duty cycle should be at least as high as the maximum duty cycle experience in use. A CW life test will result in minimum required test duration, as described in Section 5.2.

4.4.4 Monitoring Frequency

The voltage drop, V_L, across each line, the voltage, V_m, on each extrusion monitor, and the voltage, V_R, across R_B will be monitored and recorded at least once every t_m hours where,

$$t_m = \frac{t_{crit.}}{100} \qquad \text{(A-3)}$$

where $t_{crit.}$ = the critical lifetime defined in Section 5.2.

4.4.5 Failure Definition

A sample will be defined as having failed if V_L increases by 100% or more, or if V_m exceeds 10 mV.

4.4.6 Current Density

The current density must be at least as high as the maximum current density for which the metallization system is to be qualified. If a higher current density is used, the test duration may be reduced, as described in Section 5.2.

4.4.7 Duration of Test

The life test will be continued until at least fifty percent of the samples have failed or until t_m hours, whichever is smaller. The time, t_m, is given by

$$t_m = k \times t_{crit.} \qquad \text{(A-4)}$$

where $t_{crit.}$ is the required time to first failure defined in Section 5.2 and where k is plotted in Figure A-4 as a function of σ. The value of σ used to determine k is estimated using the failure times for the samples which have failed.

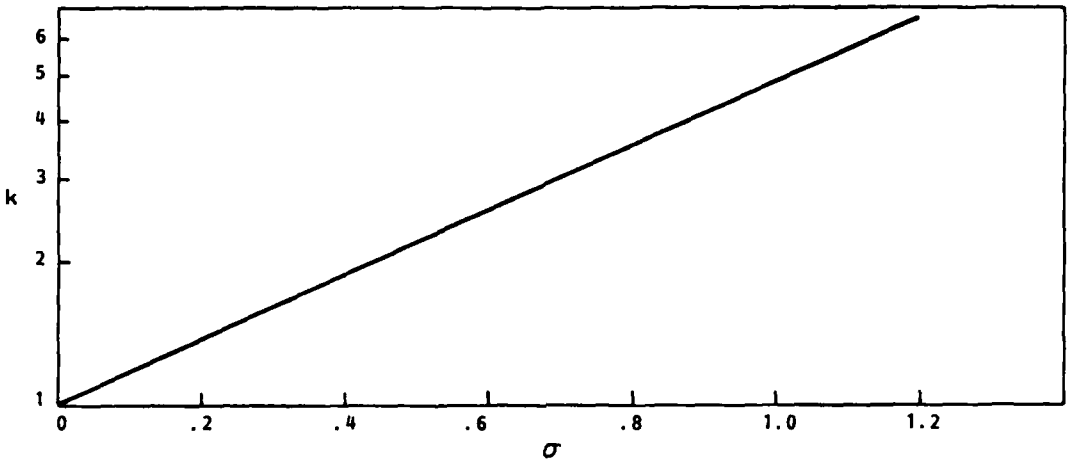

Figure A-4. Factor Determining Maximum Life Test Duration

5.0 DATA ANALYSIS/ACCEPTANCE CRITERIA

5.1 Data Analysis

The time-to-failure for each of the failed samples will be ranked in ascending order and the percentile for each sample will be calculated as

$$p = \frac{(n - 1/2) \times 100}{N} \qquad \text{(A-5)}$$

where n = the ranking of the failure (1st, 2nd, 3rd, etc.) and N = the total number of samples on test. The failure times will be plotted versus their percentiles on log-normal probability paper and the best fit straight line fitted to the data points. The value of $t_{5\%}$, i.e. the time corresponding to the fifth percentile will be estimated from the resulting distribution curve.

5.2 Acceptance Criteria

The metallization system will be considered qualified for use at current density, j_o, if the estimated value of $t_{50\%}$, obtained as described above, is larger than $t_{crit.}$ where $t_{crit.}$ is defined by

$$t_{cont.} = 1000 \left(\frac{j}{j_o}\right)^{1.5} \cdot \frac{d_o}{d} \cdot \exp\left[\frac{0.5}{k}\left(\frac{1}{T} - \frac{1}{398}\right)\right] \text{ hrs.} \qquad \text{(A-7)}$$

where j = the test current density

j_o = the maximum current density for which the metallization system is qualified ($j_o < j$)

d_o = the maximum duty cycle in use

d = the life test duty cycle

T = the metallization temperature during the life test defined in 4.3.2

and k = Boltzmann's constant.

Since the maximum duration of the life test depends on $t_{crit.}$, (Equation 4), the required duration may be controlled by the proper selection of j, d, and T.

If 50% of the samples have not failed by t_m, and if the first failure n = 1) occurred after $t_{crit.}$, the metallization system is considered qualified for use at j_o.

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